LeCroy Color Digital Oscilloscopes

LC564DL

Service Manual

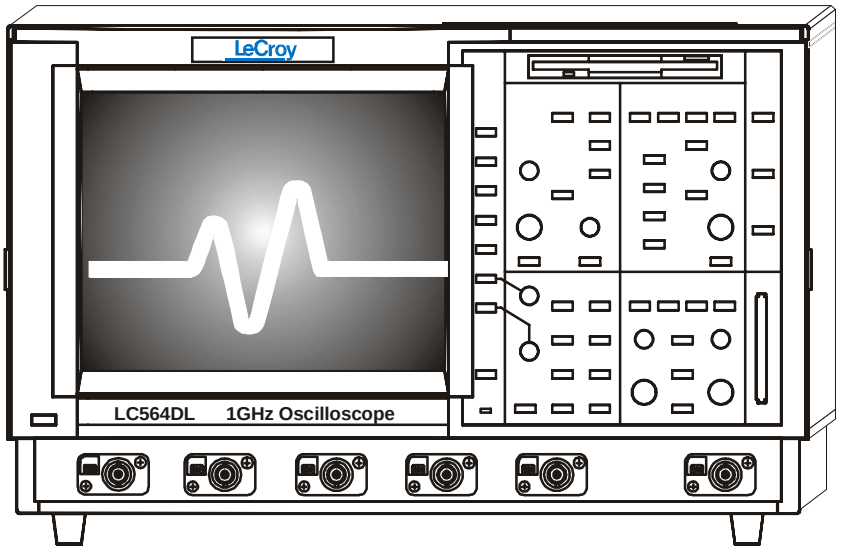

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Table of Contents

Read this first

1.	Warranty and Product Support	1-1
1.1	Warranty	1-1
1.2	Product Assistance	1-1
1.3	Maintenance Agreements	1-1
1.4	Staying Up to Date	1-2
1.5	Service and Repair	1-2
1.6	How to Return a Product	1-2
1.7	What Comes with your Scope	1-2

General Information 2-1

2.1	Product Assistance	2-1
2.2	Installation for Safe and Efficient Operation	2-1
	Operating Environment	2-1
	Safety Symbols	2-1
	Power Requirements	2-3
	Cleaning and Maintenance	2-3
	Power On	2-3

Specifications

3.1	Signal Capture	3-1
3.2	Acquisition Modes	3-2
3.3	Timebase System	3-2
3.4	Triggering System	3-2
3.5	Smart trigger Types	3-3
3.6	Autosetup	3-3
3.7	Probes	3-3
3.8	Display	3-4
3.9	Rapid Signal Processing	3-4
3.10	Waveform Processing	3-5
3.11	Interfacing	3-6
3.12	General	3-6
3.13	CE Approval	3-6

Theory of Operation

4.1	Processor Board	4-1
	MPC603e Processor	4-1
	Power Supplies	4-1
	32 bit Peripherals	4-1
	Figure 4-1: Processor Block Diagram	4-2
	DRAM	4-3
	Normal Access Timing	4-3
	Burst Access Timing	4-3
	Refresh Timing	4-3

Theory of Operation

	Memory Mapping	4-4
	VGA	4-4
	9601-2 Board: VGA proper termination	4-4
	Bus Sizer	4-5
	16 and 8-bit peripherals	4-5
	PCMCIA Interface	4-5
	Flash Prom	4-6
	NVRAM	4-6
	Interrupt Controller	4-6
	Floppy Controller	4-6
	Centronics	4-6
	Small Peripheral Interface	4-7
	Serial Interface For On Board Peripherals	4-7
	RTC	4-7
	Front Panel	4-7
	Watchdog and Reset Generation	4-8
	Bus Error Generation	4-8
	I/O Structure & GAL's Installed	4-8
	Figure 4-2: Peripheral Decoding and Data Bus Size	4-9
4.2	900079 Main Acquisition Board	4-10
4.2.1	Introduction	4-10
4.2.2	Front End	4-10
	Front End Power off State	4-11
	Figure 4-3: Front End Power off State	4-11
	50Ohm Input Direct Path	4-12
	Figure 4-4: 50Ohm Input Direct Path	4-12
	50Ohm Input Divide by 10 Path	4-12
	Figure 4-5: 50Ohm Input Divide by 10 Path	4-12
	1 MOhm Direct Path	4-13
	Figure 4-6: 1 MOhm Direct Path	4-13
	I Mohm Input Divide by 10 AC Coupled Path	4-13
	Figure 4-7: 1 Mohm Divide by 10 AC Coupled	4-13
	Front end analog controls	4-13
4.2.3	Main Acquisition Board Block Diagram	4-14
	Figure 4-8: Front End, Trigger, Sample & Hold, ADC	4-14
4.2.4	One, Two and Four Channel Mode	4-15
	Four Channel Mode	4-15
	Figure 4-9 Four Channel Mode Signal Routing	4-15
	Two Channel Mode	4-15
	Figure 4-10 Two Channel Mode Signal Routing	4-15
4.2.4	Control & Transfer Block Diagram	4-16
	Figure 4-11: Processor Control, Min/Max, Buffer Memory	4-16
4.2.5	Trigger	4-17
	Analog Controls	4-17
	TV Trigger	4-17
4.2.6	Analog to Digital Converter	4-17
	Introduction	4-17

Theory of Operation

4.2.7	Time Base	4-18
	Introduction	4-18
	Figure 4-12: Time Base Block Diagram	4-18
4.3	F9301-4 GPIB & RS232 Interface	4-19
4.3.1	GPIB/RS232 Interface Block Diagram	4-19
	Figure 4-13: GPIB/RS232 Interface Block Diagram	4-19
4.3.2	RS232 Serial Interface	4-19
4.3.3	GPIB Interface	4-19
4.4	Front Panel	4-20
4.5	F9300-7 Printer Controller	4-20
4.6	PS9611 Power Supply	4-20
4.6.1	Specifications	4-20
4.6.2	Power Supply Block Diagram	4-22

Performance Verification

5	Performance Verification Procedures	5-1
5.1	Introduction	5-1
5.1.1	List of Tested Characteristics	5-1
5.1.2	Calibration Cycle	5-1
5.2	Test Equipment Required	5-2
5.2.1	Test Records	5-2
5.3	Turn On	5-2
5.4	Input Impedance	5-3
5.4.1	Channel Input Impedance	5-3
5.4.1.a	DC 1MΩ	5-3
5.4.1.b	AC 1MΩ	5-4
5.4.1.c	DC 50Ω	5-5
5.4.2	External Trigger Input Impedance	5-6
5.4.2.a	DC 1MΩ	5-6
5.4.2.b	DC 50Ω	5-7
5.4.3	Ground	5-8
5.5	Leakage Current	5-9
5.5.1	Channel Leakage Current	5-9
5.5.1.a	DC 1MΩ	5-9
5.5.1.b	DC 50Ω	5-10
5.5.2	External Trigger Leakage Current	5-10
5.5.2.a	DC 50Ω	5-10
5.5.2.b	DC 50Ω EXT/5	5-11
5.6	Average Noise Level	5-11
5.6.1	Peak to Peak Noise	5-11
5.6.1.a	DC 1MΩ	5-11
5.6.1.b	AC 1MΩ	5-14
5.6.1.c	DC 50Ω	5-15
5.6.1.d	DC 50Ω, 2 Channel Mode	5-16

Performance Verification

5.6.2	RMS Noise	5-18
5.6.2.a	DC 1MΩ	5-18
5.6.2.b	AC 1MΩ	5-19
5.6.2.c	DC 50Ω	5-20
5.6.2.d	DC 50Ω, 2 Channel Mode	5-21
5.6.3	Ground Line Test	5-23
5.6.3.a	DC 1MΩ	5-23
5.6.3.b	DC 50Ω	5-26
5.6.3.c	DC 50Ω, 2 Channel Mode	5-27
5.7	DC Accuracy	5-28
5.7.1	Positive DC Accuracy	5-28
5.7.1.a	DC 50Ω	5-28
5.7.1.b	DC 1MΩ	5-32
5.7.2	Negative DC Accuracy	5-35
5.7.2.a	DC 50Ω	5-35
5.7.2.b	DC 1MΩ	5-36
5.8	Offset Accuracy	5-37
5.8.1	Positive Offset Accuracy	5-37
5.8.1.a	DC 50Ω	5-37
5.8.1.b	DC 1MΩ	5-40
5.8.2	Negative Offset Accuracy	5-41
5.8.2.a	DC 50Ω	5-41
5.8.2.b	DC 1MΩ	5-42
5.9	Bandwidth	5-44
5.9.1	Description	5-44
5.9.1.a	DC 50Ω	5-44
5.9.1.b	DC 50Ω with Bandwidth Limiter On	5-48
5.9.2	DC 1MΩ	5-51
5.10	Trigger Level	5-54
5.10.1	Description	5-54
5.10.2	Channel Trigger at 0 Division Threshold	5-54
5.10.3	Channel Trigger at +3 Divisions Threshold	5-57
5.10.4	Channel Trigger at –3 Divisions Threshold	5-58
5.10.5	External Trigger at 0 Division Threshold	5-60
5.10.6	External Trigger at +3 Divisions Threshold	5-62
5.10.7	External Trigger at –3 Divisions Threshold	5-63
5.10.8	External/5 Trigger at 0 Division Threshold	5-64
5.10.9	External/5 Trigger at +3 Divisions Threshold	5-66
5.10.10	External/5 Trigger at –3 Divisions Threshold	5-67
5.11	Smart Trigger	5-68
5.11.1	Trigger on Pulse Width 10 nsec	5-68
5.11.1.a	Pulse Width < 10 nsec	5-68
5.11.1.b	Pulse Width > 10 nsec	5-68
5.11.2	Trigger on Pulse Width 100 nsec	5-70

Performance Verification

5.11.2.a	Pulse Width < 100 nsec	5-70
5.11.2.b	Pulse Width > 100 nsec	5-70
5.12	Time Base Accuracy	5-71
5.12.1	Description	5-71
5.12.2	500 MHz Clock Verification Procedure	5-71
5.13	Overshoot and Rise time	5-73
5.13.a	DC 50Ω	5-73
5.13.b	DC 1MΩ	5-75

Test Record

Table 1	LC684D Performance Certificate	1 of 12
Table 2	Impedance Test Record	2 of 12
Table 3	Leakage Voltage Test Record	2 of 12
Table 4	Peak to Peak Noise Test Record	3 of 12
Table 5	RMS Noise Test Record	3 of 12
Table 6	DC 1MΩ Ground Line Test Record	4 of 12
Table 7	DC 50Ω Ground Line Test Record	4 of 12
Table 8	DC 50Ω Positive DC Accuracy Test Record	5 of 12
Table 9	DC 1MΩ Positive DC Accuracy Test Record	6 of 12
Table 10	DC 50Ω Negative DC Accuracy Test Record	7 of 12
Table 11	DC 1MΩ Negative DC Accuracy Test Record	7 of 12
Table 12	Positive Offset Test Record	7 of 12
Table 13	Negative Offset Test Record	8 of 12
Table 14	DC 50Ω, 50 mv/div. Bandwidth Test Record	8 of 12
Table 15	DC 50Ω, 100 mv/div. Bandwidth Test Record	9 of 12
Table 16	DC 50Ω, Bandwidth Limiter Test Record	9 of 12
Table 17	DC 1MΩ, Bandwidth Test Record	10 of 12
Table 18	Channel DC Trigger Test Record	10 of 12
Table 19	External & Ext/5 DC Trigger Test Record	11 of 12
Table 20	Smart Trigger Test Record	12 of 12
Table 21	Time Base Test Record	12 of 12
Table 22	Rise time and Overshoot Test Record	12 of 12

Maintenance

6.1	Introduction	6-1
6.1.1	Safety Precautions	6-1
6.1.2	Antistatic Precautions	6-1
6.2	Disassembly and Assembly Procedure	6-2
6.2.1	Disassembly Procedure	6-2
6.2.1.a	Removal of the Front Bezel	6-2
6.2.1.b	Removal of the Upper Cover Assembly	6-2
6.2.1.c	Removal of the Front Frame with Color Monitor	6-3
6.2.1.d	Removal of the Processor Board	6-3
6.2.1.e	Removal of the Power Supply Assembly	6-3
6.2.1.f	Removal of the Upper Shield Assembly	6-4
6.2.1.g	Removal of the Rear Panel Assembly	6-4
6.2.1.h	Removal of the Main Board Assembly	6-4
6.2.2	Assembly Procedure	6-5
6.3	Software Update Procedure	6-6
6.3.1	Upgrading Firmware	6-6
6.3.1.a	Performing the Update from GPIB	6-6
6.3.1.b	Performing the Update from RS232	6-7
6.3.1.c	Performing the Update from Floppy	6-8
6.3.2	Software Options	6-8
6.3.2.1	Changing Software Option Key	6-9
6.3.2.1.a	Scope ID, Scope Serial Number	6-9
6.3.2.1.b	Entering Option Key	6-9
6.3.3	Processor Board Exchange Procedure	6-9
6.4	Equipment and Spare Parts Recommended for Service	6-10
6.4.1	Test Equipment Required	6-10
6.4.2	Spare Parts Recommended for Service	6-10
6.5	Calibration Procedures	6-10
6.5.1	Power Supply Calibration Procedure	6-11
6.6	Troubleshooting and Flow Charts	6-12
6.6.1	Introduction	6-12
6.6.2	Line Fuses Replacement	6-12
6.6.3	Initial Troubleshooting Chart	6-12
6.6.4	Fan Problem	6-14
6.6.5	Power Supply Voltages Problem	6-15
6.6.6	Display Problem	6-16
6.6.7	Front Panel Controls Do not Operate	6-17
6.6.8	Remote Control GPIB & RS232 Problem	6-18
6.6.9	Performance Verification Fails	6-19
6.6.10	Floppy Disk Drive Problem	6-20
6.6.11	Graphic Printer Problem	6-21
6.6.12	Centronics Problem	6-22
6.6.13	Hard Disk Drive Problem	6-23

Replaceable Parts

LC684D, LC684DM, LC684DL & LC684DXL	7-1
9615-GP01 Graphic Printer Assembly	7-2
F9300-7 Printer Controller	7-2
F9300-8 Hard Disk Interface	7-4
F9301-4 GPIB & RS232 Interface	7-5
F9601-11-16 Processor with 16 Mbytes Memory	7-5
F9601-11-64 Processor with 64 Mbytes Memory	7-5
S9601-11 Processor Card without DRAM Memory	7-6
F9601-2 Centronics & VGA Interface	7-8
F9601-6 Floppy Disk Drive Assembly	7-9
F9601-8 Main Switch Board	7-9
F9602-1-64 Processor Card 200 Mhz With DRAM	7-9
S9602-1 Processor 200MHz Card Without DRAM	7-9
F9602-9 Universal Fan Control	7-12
F9615-3 Main Acquisition Board	7-12
S9615-3 Main Acquisition Board	7-13
F9615-5 Keyboard Assembly	7-19
LC684-ACC Accessories	7-20
LC684-CKTRIG Option	7-20
LCDFP9615 LCD Display and Front Panel Assembly	7-21
LCLC9615 Lower Cover	7-21
LCXXX-PAK Packaging Material	7-21
M9615 Mechanical Parts	7-22
RP9615 Rear Panel Assembly	7-22
S9615-21 Buffer Board	7-23
S9615-22 Interface Circuit	7-23
S9615-51 Keypad	7-23
S9615-52 Generic Front Panel	7-24
UC9615 Upper Cover Assembly	7-24
US9615 Upper Shield Rod Assembly	7-24

Mechanical Parts

Figure 8-1: LC684D/DM/DL/DXL Cabinet 8-1
Figure 8-2 LC684D/DM/DL/DXL Chassis Assembly 8-2
Cabinet Replaceable Parts 8-3
Chassis Replaceable Parts 8-3
Figure 8-3: Power Supply Installation 8-4
Figure 8-4: LC684D Lower Cover Assembly 8-5
Power Supply Installation Replaceable Parts 8-6
Lower Cover Replaceable Parts 8-6
Figure 8-5: Lower Cover with CKTRIG Option 8-7
Figure 8-6: Lower Cover 8-8
Lower Cover with CKTRIG Option Replaceable Parts 8-9
Lower Cover Replaceable Parts 8-9
Figure 8-7: CKTRIG Option 8-10
Figure 8-8: Rear Panel Assembly 8-11
CKTRIG Option Replaceable Parts 8-12
Rear Panel Replaceable Parts 8-12
Figure 8-9: F9615-3 Main Board Assembly 8-13
Figure 8-10: Main Board Assembly 8-14
F9615-3 Main Board Replaceable Parts 8-15
Figure 8-11: Upper Shield Assembly 8-16
Figure 8-12: Front Frame Assembly 8-17
Upper Shield Replaceable Parts 8-18
Front Frame Replaceable Parts 8-18
Figure 8-13: Keypad Assembly 8-19
Figure 8-14: Fan Assembly 8-20
Keypad Replaceable Parts 8-21
Fan Replaceable Parts 8-21
Figure 8-15: Graphic Printer Assembly 8-22
Figure 8-16: Upper Cover Assembly 8-23
Graphic Printer Replaceable Parts 8-24
Upper Cover Replaceable Parts 8-24
Figure 8-17: Hard Disk Assembly 8-25
Figure 8-18: Centronics & VGA Interface Assembly 8-26
Figure 8-19: Floppy Disk Assembly 8-27
Hard Disk Replaceable Parts 8-28
Centronics & VGA Replaceable Parts 8-28
Floppy Replaceable Parts 8-28
Figure 8-20 LC684D Dimensions 8-29
Figure 8-21: :C684D Packaging 8-30

Schematics, Layouts, Parts List

F9300-7 Graphics Printer Controller Schematic	9-2
F9300-7 Graphics Printer Controller Layout	9-4
F9300-7 Graphics Printer Controller Parts List	9-5
F9300-8 Hard Disk Interface Schematic	9-7
F9300-8 Hard Disk Interface Layout	9-8
F9300-8 Hard Disk Interface Parts List	9-9
F9301-4 GPIB & RS232 Interface Schematic	9-10
F9301-4 GPIB & RS232 Interface Layout	9-12
F9301-4 GPIB & RS232 Interface Parts List	9-13
F9601-11-X Processor Schematic	9-14
F9601-11-X Processor Layout	9-23
F9601-11-X Processor Parts List	9-25
F9601-2NY Centronics and VGA Interface Schematic	9-31
F9601-2NY Centronics and VGA Interface Layout	9-32
F9601-2NY Centronics and VGA Interface Parts List	9-33
F9601-61 Floppy Adapter Schematic	9-34
F9601-61 Floppy Adapter Layout	9-35
F9601-8NY Main Switch Board Schematic	9-36
F9601-8NY Main Switch Board Layout	9-37
F9601-61 Floppy Adapter Parts List	9-38
F9601-8NY Main Switch Board Parts List	9-38
F9602-1-X 200 MHz Processor Schematic	9-39
F9602-1-X 200 MHz Processor Layout	9-49
F9602-1-X 200 MHz Processor Parts List	9-51
F9602-9 Universal Fan Controller Schematic	9-57
F9602-9 Universal Fan Controller Layout	9-59
F9602-9 Universal Fan Controller Parts List	9-61
S9615-3 Main Acquisition Board Schematic	9-63
S9615-3 Main Acquisition Board Layout	9-123
S9615-3 Main Acquisition Board Parts List	9-161
S9615-21 Buffer Board Schematic	9-190
S9615-21 Buffer Board Layout	9-191
S9615-21 Buffer Board Parts List	9-192
S9615-22 Interface Circuit Schematic	9-193
S9615-22 Interface Circuit Layout	9-194
S9615-51 Keypad Schematic	9-195
S9615-51 Keypad Layout	9-196
S9615-22 Interface Circuit Parts List	9-197
S9615-51 Keypad Parts List	9-197
S9615-52 Generic Front Panel Schematic	9-198
S9615-52 Generic Front Panel Layout	9-199
S9615-52 Generic Front Panel Parts List	9-200

1. Warranty and Product Support

It is recommended that you thoroughly inspect the contents of the oscilloscope packaging immediately upon receipt. Check all contents against the packing list/invoice copy shipped with the instrument. Unless LeCroy is notified promptly of any missing or damaged item, responsibility for its replacement cannot be accepted. Contact your nearest LeCroy Customer Service Center or national distributor immediately (see chapter 2 for *contact numbers*).

1.1 Warranty

LeCroy warrants its oscilloscope products for normal use and operation within specifications for a period of three years from the date of shipment. Calibration each year is recommended to ensure in-spec. performance. Spares, replacement parts and repairs are warranted for 90 days. The instrument's firmware has been thoroughly tested and is thought to be functional, but is supplied without warranty of any kind covering detailed performance. Products not made by LeCroy are covered solely by the warranty of the original equipment manufacturer.

Under the LeCroy warranty, LeCroy will repair or, at its option, replace any product returned within the warranty period to a LeCroy authorized service center. However, this will be done only if the product is determined after examination by LeCroy to be defective due to workmanship or materials, and not to have been caused by misuse, neglect or accident, or by abnormal conditions or operation.

1.2 Product Assistance

***Note:** This warranty replaces all other warranties, expressed or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract or otherwise. The client will be responsible for the transportation and insurance charges for the return of products to the service facility. LeCroy will return all products under warranty with transport prepaid.*

Help on installation, calibration, and the use of LeCroy equipment is available from the LeCroy Customer Service Center in your country.

1.3 Maintenance Agreements

LeCroy provides a variety of customer support services under Maintenance Agreements. Such agreements give extended warranty and allow clients to budget maintenance costs after the initial three-year warranty has expired. Other services such as installation, training, enhancements and on-site repairs are available through special supplemental support agreements.

1.4 Staying Up to Date

LeCroy is dedicated to offering state-of-the-art instruments, by continually refining and improving the performance of LeCroy products. Because of the speed with which physical modifications may be implemented, this manual and related documentation may not agree in every detail with the products they describe. For example, there might be small discrepancies in the values of components affecting pulse shape, timing or offset, and — infrequently — minor logic changes. However, be assured the scope itself is in full order and incorporates the most up-to-date circuitry. LeCroy frequently updates firmware and software during servicing to improve scope performance, free of charge during warranty. You will be kept informed of such changes, through new or revised manuals and other publications.

Nevertheless, you should retain this, the original manual, for future reference to your scope's unchanged hardware specifications.

1.5 Service and Repair

Please return products requiring maintenance to the Customer Service Department in your country or to an authorized service facility. The customer is responsible for transportation charges to the factory, whereas all in-warranty products will be returned to you with transportation prepaid. Outside the warranty period, you will need to provide us with a purchase order number before we can repair your LeCroy product. You will be billed for parts and labor related to the repair work, and for shipping.

1.6 How to return a Product

Contact the nearest LeCroy Service Center or office to find out where to return the product. All returned products should be identified by model and serial number. You should describe the defect or failure, and provide your name and contact number. In the case of a product returned to the factory, a Return Authorization Number (RAN) should be used.

Return shipments should be made prepaid. We cannot accept COD (Cash On Delivery) or Collect Return shipments. We recommend air-freighting.

It is important that the RAN be clearly shown on the outside of the shipping package for prompt redirection to the appropriate LeCroy department.

1.7 What Comes with Your Scope

The following items are shipped together with the standard configuration of this oscilloscope:

- Front Scope Cover
- 10:1 10 MΩ PP005 Passive Probe — *one per channel*
- *PP096 8GS/s adapter*
- *Two* 250 V Fuses, AC Power Cord and Plug
- *Operator's Manual* , *Remote Control Manual, Hands-On Guide*
- Performance Certificate or Calibration Certificate, Declaration of Conformity

Note: Wherever possible, please use the original shipping carton. If a substitute carton is used, it should be rigid and packed so that that the product is surrounded by a minimum of four inches or 10 cm of shock-absorbent material.

2. General Information

2.1 Product Assistance

Help on installation, calibration, and the use of LeCroy equipment is available from your local LeCroy office, or from LeCroy's

- Customer Care Center, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977–6499, U.S.A., tel. (914) 578–6020
- European Service Center, 2, rue du Pré-de-la-Fontaine, 1217 Meyrin 1, Geneva Switzerland, tel. (41) 22/719 21 11.
- LeCroy Japan Corporation, Sasazuka Center Bldg – 6th floor, 1-6, 2-Chome, Sasazuka, Shibuya-ku, Tokyo Japan 151-0073, tel. (81) 3 3376 9400

2.2 Installation for Safe and Efficient Operation

Operating Environment

The oscilloscope will operate to its specifications if the environment is maintained within the following parameters:

Temperature .....5 to 40 °C (41 to 104 °F) rated.

Humidity .....Maximum relative humidity 80 % RH (non-condensing) for temperatures up to 31 °C decreasing linearly to 50 % relative humidity at 40 °C

Altitude .....2000 m (6560 ft)

The oscilloscope has been qualified to the following EN61010-1 category:

Installation (Overvoltage) CategoryII

Pollution Degree 2

Safety Symbols

Where these symbols or indications appear on the front or rear panels, and in this manual, they have the following meanings:

..... **CAUTION**: Refer to accompanying documents (for Safety-related information). *See elsewhere in this manual wherever the symbol is present,as indicated in the Table of Contents*.

..... **CAUTION**: Risk of electric shock

..... **On (Supply)**

 Off (Supply)

..... Earth (Ground) Terminal

..... **Protective Conductor Terminal**

..... **Earth (Ground) Terminal on BNC Connectors**

WARNING ..... **Denotes a hazard. If a WARNING is indicated on the instrument, do not proceed until its conditions are understood and met.**

Any use of this instrument in a manner not specified by the manufacturer may impair the instrument's safety protection.

The oscilloscope has *not* been designed to make direct measurements on the human body. Users who connect a LeCroy oscilloscope directly to a person do so at their own risk.

Power Requirements

The oscilloscope operates from a 115 V (90 to 132 V) or 220 V (180 to 250 V) AC power source at 45 Hz to 66 Hz. No voltage selection is required, since the instrument automatically adapts to the line voltage present.

The power supply of the oscilloscope is protected against short-circuit and overload by means of two 6.3 A/250 V AC, “T” rated fuses (size: 5 X 20 mm), located above the mains plug. Disconnect the power cord before inspecting or replacing a fuse. Open the fuse box by inserting a small screwdriver under the plastic cover and prying it open.

For continued fire protection at all line voltages, replace only with fuses of the specified type and rating (T 6.3 A/250 V).

Maintain the ground line to avoid an electric shock.

None of the current-carrying conductors may exceed 250 V rms with respect to ground potential. The oscilloscope is provided with a three-wire electrical cord containing a three-terminal polarized plug for mains voltage and safety ground connection.

The plug's ground terminal is connected directly to the frame of the unit. For adequate protection against electrical hazard, this plug must be inserted into a mating outlet containing a safety ground contact.

Cleaning And Maintenance

Maintenance and repairs should be carried out exclusively by a LeCroy technician (*see* Chapter 2). Cleaning should be limited to the exterior of the instrument only, using a damp, soft cloth. Do not use chemicals or abrasive elements. Under no circumstances should moisture be allowed to penetrate the oscilloscope. To avoid electric shocks, disconnect the instrument from the power supply before cleaning.

Risk of electrical shock: No user serviceable parts inside. Leave repair to qualified personnel.

Power On

Connect the oscilloscope to the power outlet and switch it on by pressing the power switch located on the rear panel. After the instrument is switched on, auto-calibration is performed and a test of the oscilloscope's ADCs and memories is carried out. The full testing procedure takes approximately 10 seconds, after which time a display will appear on the screen.

3. LC564DL Specifications

3.1 Signal Capture

Acquisition System

Bandwidth (-3 dB):
@ 50Ω: DC to 1 GHz
@ 1 MΩ DC: Bandwidth dependent on probe used
No. of Channels: 4
Sample Rate: 2 GS/s (4 ch); 4 GS/s (2 ch)
Sensitivity:
50Ω : 2 mV/div to 1 V/div
1MΩ : 2 mV/div to 2 V/div
Scale factors: Choice of over 12 probe attenuation factors selectable via front panel menus.
Offset Range:
2.0 - 4.99 mV/div: ±400 mV
5.0 - 99 mV/div (50Ω only) : ±1 V
5.0 - 100 mV/div (1 MΩ only) : ±1 V
0.1 - 1.0V/div (50Ω only): ±10 V
102 mv - 2.0V/div (1 MΩ only): ±20 V
±20 V across the whole sensitivity range when using the AP020/AP022 FET probe.
DC Accuracy: typical ± 2% of full scale + 1% offset setting.
Vertical Resolution: 8 bits.
Bandwidth Limiter: 25 MHz, or 200MHz user selectable
Input Coupling: AC (> 10Hz typ.), DC, GND.
Input Impedance: 10MΩ//11pF (system capacitance using PP005) or 50 Ω ±1.25%.
Max Input: 50Ω: ±5V DC (500mW) or 5V RMS.
1MΩ: 100 V (DC+ peak AC ≤10 kHz).

Acquisition System Configuration

Active Channels	Maximum Sample Rate	Maximum Record Length
4	2 GS/s	1 M
2	4 GS/s	2 M
1	4 GS/s	2 M

3.2 Acquisition Modes

Random Interleaved Sampling (RIS): 25GS/s.
For repetitive signals from 200 ps/div to 1 µs/div.
Single shot: For transient and repetitive signals from 1 ns/div (2 Ch), 2 ns/div (4Ch)
Sequence: Stores multiple events- each of them time stamped- in segmented acquisition memories.
Dead Time Sequence mode: Typically 30 µs
Number of segments available 2-2000,

3.3 Timebase System

Timebases: Main and up to 4 Zoom Traces.
Time/Div Range: 1ns/div (at 4 GS/s), 2ns/div (at 2 GS/s) to 1,000 s/div.
Clock Accuracy: ≤10 ppm.
Interpolator resolution: 10 ps.
Roll Mode in normal trigger mode: 500 ms to 1,000 s/div.
External Clock: Optional (CKTRIG) Zero crossing level DC to 500 MHz rear panel fixed frequency clock input (<20 ns rise/falltime)
External Reference: Optional (CKTRIG) 10 MHz rear-panel input.

3.4 Triggering System

Trigger Modes: Normal, Auto, Single, and Stop.
Trigger Sources: CH1, CH2, CH3, CH4, Line, Ext, Ext/5. Slope.
Level and Coupling are unique for each source.
Slope: Positive, Negative, Bi-Slope (Window in & out)
Coupling: AC (-3db at <10Hz), DC, HF (175 MHz to 1GHz), LFREJ (>50KHz), HFREJ (<100MHz).
Pre-trigger recording: 0 to 100% of full scale (adjustable in 1% increments).
Post-trigger delay: 0 to 10,000 divisions (adjustable in 0.1 div increments).
Holdoff by time: 2 ns to 20 s.
Holdoff by events: 1 to 99,999,999.
Internal Trigger Range: ±5 div.
Maximum Trigger Frequency: 1 GHz (DC, AC), > 1.5 GHz (HF)
EXT Trigger Max Input: 1MΩ//20pF: 100V (DC + peak AC≤ 10kHz)
50Ω ±3%: ±5 V DC (500 mW) or 5 V RMS.
EXT Trigger Range: ±0.5 V (±2.5 V with Ext/5).
Trigger Output: Optional ECL rear panel output (option CKTRIG). The calibrator output can provide a trigger status or a Pass/Fail test output.

3.5 Smart Trigger Types

Pattern: Trigger on the logic combination of 5 inputs - CH1, CH2, CH3, CH4 and EXT Trigger, where each source can be defined as High, Low or Don't Care. The Trigger can be defined as the beginning or end of the specified pattern
Signal or Pattern Width: Trigger on glitches as short as 600 ps or on pulse widths Within/outside two limits selectable from 600 ps to 20 s.
Slew Rate: Trigger on rising, falling edges within/outside two time limits selectable from 600 ps to 20 s.
Signal or Pattern Interval: Trigger on an interval between two limits selectable from 2ns to 20s.
Dropout: Trigger if the signal drops out for longer than a time-out from 2 ns to 20s.
Runt: Trigger on positive or negative Runts within/outside two limits selectable from 600 ps to 20 s.
State/Edge Qualified: Trigger on any source only if a given state (or transition) has occurred on another source. The delay between these events can be defined as a number of events on the trigger channel or as a time interval.
TV: Allows selection of up to 1500 lines and field synchronization for PAL, SECAM, NTSC or non-standard video
Exclusion Triggering: Trigger on intermittent faults by specifying the normal width, period, risetime or amplitude of a signal.
The oscilloscope will trigger only on aberrations.

3.6 Autosetup

Automatically sets sensitivity, vertical offset and timebase on all display channels.

Autosetup Time: Approximately 3 seconds.
Vertical Find: Automatically sets sensitivity and offset for selected channel.

3.7 Probes

Model: One PP005 probe is supplied per channel. DC to 500 MHz typical at probe tip, 500 V max.
Optional Probes: 2.5 Ghz FET probe AP022, 1 GHz FET probe (AP020); 1 GHz active differential probe (AP034), 500 MHz active differential probe (AP033).

Probe calibration: Max 1 V into 1 MΩ, 500 mV into 50 Ω, frequency and amplitude programmable, pulse or square wave selectable, rise and fall time 1 ns typical. Alternatively, the Calibrator output can provide a trigger output or a Pass/Fail test output.

3.8 Display

Type: Color 10.4" TFT-LCD.
Resolution: VGA (640X480 pixels)
Display Area: 212mm x 160mm
Controls: Menu controls for brightness and color selection.
Grid Styles: Single, Dual, Octal, XY, Single+XY, Dual+XY, and Full Screen
An enlarged view of each grid style.
Graticules: Internally generated; separate intensity control for grids and waveforms. Selectable blending of grid with displayed traces.
Waveform Style: Dot-joint with optional sample point highlight or Dots-only.
Persistence Modes: Color-graded persistence and Analog Persistence, infinite or variable with decay over time. In color-graded persistence, a color spectrum from red through violet is used to map signal intensity. With Analog Persistence, the brightness level of a single color denotes signal intensity. Each trace's persistence data is stored in 64K levels.
Trace Display: Opaque or transparent mode, with overlap management.
Number of Traces: 8 (supports a mix of channels, memories or math functions).
Real-time Clock: Date, hours, minutes, seconds.
External Monitor: Rear panel 15-pin socket for VGA compatible monitor.
Vertical Zoom: Up to 5x Vertical Expansion (50x with averaging, up to 40 μV/div sensitivity).
Horizontal Zoom: Waveforms can be expanded to 0.4 points/division.
Auto Scroll: Use Auto Scroll to automatically "Play" the captured signal to identify anomalies quickly and easily. With a selectable zoom expansion and scrolling speed, you can set up Auto Scroll to match your signal viewing needs.
The scrolling speed can be adjusted during the scan to focus on the more interesting characteristics of the signal.
"REVERSE" enables you to quickly review any part of the signal.

3.9 Rapid Signal Processing

Microprocessor: 96 MHz PowerPC 603e
System RAM: 16 Mbytes
Video Memory: 1 Mbyte
Persistence Data Map Memory: 16 bits per displayed pixel (64k levels).

3.10 Waveform Processing

Up to four processing functions may be performed simultaneously. Functions available are: Add, Subtract, Multiply, Divide, Negate, Identity, Summation Averaging, Sine x/x, Integral, Derivative, Square Root, Ratio, Absolute Value and the advanced functions listed below.

Average: Summed averaging up to one million sweeps.
Extrema: Roof, Floor, or Envelope values up to one million sweeps.
ERES: Low-Pass digital filters provide up to 11-bit vertical resolution. Sampled data is always available, even when a trace is turned off.
FFT: Spectral Analysis with four windowing functions and FFT averaging.
Statistical Diagnostics: The Parameter Analysis package permits in-depth diagnostics on waveform parameters. Live histogramming and trending of any waveform parameter measurement is possible. The histogram can be auto-scaled to display the center and width of the distribution. This package is only standard on the LC584 Series.

Internal Memory

Waveform Memory: Up to four 16-bit memories (M1, M2, M3, M4).
Zoom & Math Memory: Up to four 16-bit Waveform Processing memories (A,B,C,D), whose length corresponds to the length of the channel acquisition memory.
Setup Memory: Four non-volatile memories. The floppy drive and optional cards or disks may also be used for high-capacity waveform and setup storage.

Cursor Measurements

Relative Time: A pair of arrow cursors measures time differences and voltage differences relative to each other.
Relative Voltage: A pair of line cursors measures voltage differences relative to each other.
Absolute Time: A cross-hair marker measures time relative to the trigger and voltage with respect to ground.
Absolute Voltage: A reference bar measures voltage with respect to ground.

PASS/FAIL:
Pass/Fail testing allows any five items (parameters and/or masks) to be tested against selectable thresholds. Waveform Limit Testing is performed using Masks which may be defined either inside the instrument or by downloading templates created on a PC. Any failure will cause pre-programmed actions, such as Hardcopy, Save to Internal Memory, Save to mass storage device (card or disk), GPIB SRQ or Pulse Out.

3.11 Interfacing

Remote Control: All front-panel controls as well as all internal functions are possible by GPIB and RS-232-C.
RS-232-C Port (Standard): Asynchronous up to 115.2 kBaud for computer/terminal control or printer/plotter connection.
GPIB Port (Standard): (IEEE-488.2) Configurable as talker/listener for computer control and fast data transfer.
Centronics Port (Standard): Hard copy parallel interface.
Hard copy: Screen dumps are activated by a front-panel button or via remote control.
Supported printers:
B/W: LaserJet, DeskJet, Epson
Color: DeskJet 550C, Epson Stylus, Canon 200/600/800 series.
An optional, internal high-resolution graphics printer is also available for screen dumps; strip-chart output formats up to 2 m/div are achievable.
Hard Copy Formats: TIFF b/w, TIFF color, BMP color and
BMP compressed.
Output Formats:
The ASCII waveform output and is compatible with spreadsheets, MATLAB, MathCad. Binary output is also available.

3.12 General

Auto-calibration Ensures specified DC and timing accuracy.
Recommended Factory Calibration Interval: 1 year
Temperature: 5° to 40°C rated accuracy (41° to 104°F).
0° to 45°C operating (32° to 113°F).
Humidity: <80% non-condensing.
Altitude: Up to 2000 m (operating), 12,000 m (non-operating).
Shock and Vibration: Conforms to selected sections of MIL-PRF-28800F,Class 3.
Power: 90-250 V AC, 45-66 Hz, 350 VA
Battery Backup: Front-panel settings maintained for two years.
Dimensions:(HWD) 10.4" x 15.65" x 17.85", 264 mm x 397 mm x 453 mm
Weight: Typ. 16 kg (35 lbs) net, typ. 24 kg (53 lbs) shipping.
Warranty: Three years.

3.13 CE Approval

EMC: Conforms to EN50081-1 (Emissions) and EN50082-1 (Immunity)
Safety: The oscilloscope has been designed to comply with EN61010-1 Installation Category (Over-voltage category) II, 300V, Pollution degree 2.
UL and cUL approval: UL Standard: UL 3111-1; cUL Canadian Standard CSA-C22.2 No. 1010. 1-92.

4. Theory of Operation

4.1 Processor Board : F9601-11-16

MPC603e Processor

This processor board is based on the Power MPC603e processor.
It is a 64-bit RISC processor with 2x32kbyte cache. It features high speed processing and fast memory accesses.
The F9601-11-16 processor is set to an internal clock of 96MHz and is used in a 32-bit mode.

There are two “worlds” on the board:

- the 32-bit world, including the main PowerPC processor, the dynamic RAM modules and the VGA interface;
- the 8 or 16-bit world, including all other on-board peripherals, external small peripherals and acquisition board.

A MC68150 dynamic bus sizer is used as an interface between the two worlds.

Power Supplies

The board uses three power supplies from the main acquisition board: Vcc, +15V and -15V. Vee is wired on a connector for board test purposes.
The +15V supply OP-amps on the 9601-11 board, and +15V and -15V supply small peripherals.
The current processor needs a 3.3V power supply, all the rest of the logic needs 5V. All signals are TTL compatible.
The PLL circuit (88916) generates a PLL_LOCK signal, which is used to clamp the 3.3V and 2.5V references as long as the 32MHz clock is not stable. The processor also needs to be protected against too big voltage differences between 2.5V and 3.3V (diodes on the reference).
An OP-amp and a MOSFET transistor for each power supply are used. The reference voltages are taken directly from the 5V power supply by a resistive divider.
Capacitors and a few diodes ensure that the supplies do not exceed dangerous levels at power-up, nor rise too fast.

32-bit Peripherals

There are only three devices hooked up on to the processors 32-bit data bus:

- the VGA video controller
- the DRAM system
- the bus sizer, bridge to the 68k-like world

Processor Block Diagram

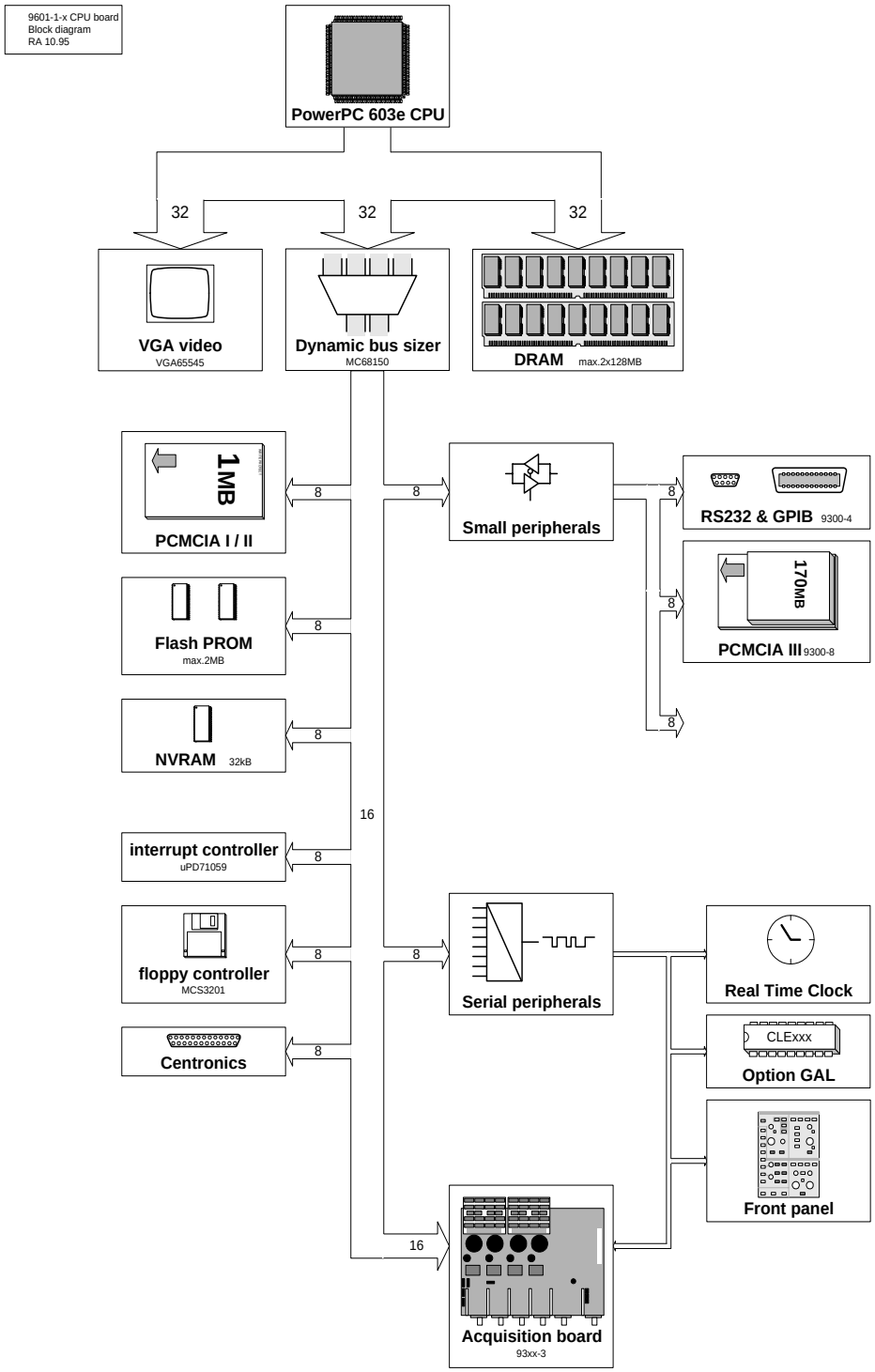


Fig 4-1: 9601-11 Block diagram

DRAM

The DRAM consists of two SIMM modules from 4 MB up to 32 MB each.
By interleaving two SIMMs, the access time is dramatically reduced (one beat every 30ns, while the other module “recovers” from the previous access).
The DRAM control logic, including refresh control, is built around several GALs and a few gates.
RAMEUR (A44) is the main sequencer. It inserts refresh cycles whenever needed, and drives row and column addressing timing.
RASADE (A39) controls the row address select lines of the memory modules, and generates the addresses for double beat or burst accesses.
OCCASE (A37) generates the column address select lines of the SIMMs.
DRAME (A57) holds some glue logic, and a state machine that counts the number of beats, inserting pauses in the access if necessary (single SIMM support).
Four multiplexers (A40, 42, 46 and 47) switch between odd and even addresses to be sent to the address lines of the modules. One more multiplexer (A38) switches low order address bits, routing them either directly to the processor, or to the DRAM address generator in RASADE.

Normal Access Timing

This is the simplest access possible: the processor puts an address onto the address bus, and reads back or writes one long word (32-bit wide) to DRAM. Depending on the address (odd or even), bank A or bank B is selected in a dual SIMM configuration.

Burst Access Timing

A burst access on a 603e configured as a 32-bit device, consists of either two (“double beat”) or eight (“burst”) successive reads in DRAM. The idea is to put a start address onto the address bus, and read back or write several data’s from or to DRAM every clock cycle, without the processor incrementing the address (this is done by the external logic). To increase system performance, the memory has been interleaved, allowing each module to access a memory location every 60ns, but with a delay of 30ns between the modules.
A burst access is signaled by an active low _TBST signal and a 32-bit access (SIZ2..0= 011), a double-beat access is indicated by a high _TBST but an access size of 64 bits (SIZ2..0= 100). The double-beat case is decoded by a GAL (VIADUC), and the signal is named _DBEAT (active low).

Refresh Timing

The 32 kHz clock from the real time clock chip is used to refresh periodically the DRAM.
The GAL RAMEUR generates the refresh cycles, as well as the sequencing of _RAS and _CAS. Depending on the operating mode, it chooses to access slot A or selects alternately slots A and B.

Memory Mapping

By default, the board is set to the biggest memory size possible. The software checks out for “holes” in the addressing space, and sets accordingly two configuration lines, MAP1 and MAP0.

MAP1..0	meaning
00	2x4, single sided SIMMs
01	2x8 MB SIMMs
10	2x32 MB SIMMs

VGA

The VGA 65545 controller chip (A27) includes its own address decoding logic. It generates all video signals (red, green and blue video, horizontal and vertical syncs, and all control lines to drive a flat panel) and controls its associated 1 MB video dynamic RAM (reads, write and refresh cycles).
All timings are extracted from the 16 MHz bus clock, so no external crystal or timebase is needed.

The horizontal and vertical sync. signals are sent to both the internal and the external video connector (high density DB15 on the 9601-2 board). The external syncs are direct, the internal syncs pass through the GAL VIADUC (A32), allowing to force these two lines to ground. This puts the internal display in power down mode (standby mode).
The chip can support several bus interfaces (PCI, ISA, VL,), it is configured as VL-bus.

The 65545 chip generates red, green and blue video signals. These are controlled-impedance lines (37.5 Ohm approximately, which corresponds to two 75 Ohm loads in parallel). A low-pass filter is implemented right at the outputs from the VGA controller, and another low-pass filter is located at each video connector on the 9601-2 board (just after the “active” load).

9601-2 Board: VGA proper termination (auto termination)

The 9601-2 board is a complement to the 9601-11 main processor board. It holds the external Centronics connector (female DB-25) with its EMI filters, both internal and external VGA connectors (female mini DB-15), and line termination for R, G and B signals.

The VGA controller is able to drive a load of 37.5 Ohms on its Red, Green and Blue outputs (two 75 Ohms loads in parallel). The line impedance of these signals on the processor board is therefore close to 37.5 Ohms. The 9601-2 board includes a special termination circuit that keeps the loads on the R, G and B lines at 37.5 Ohms, no matter if one or two 75 Ohms loads are connected. The circuit assumes that a 75 Ohms load is present on each output.

Bus Sizer

The MPC603e processor does not support dynamic bus sizing, as did the 68k family. Many parts of the software and the hardware rely on that feature. A Motorola MC68150 chip ‘translates’ the PowerPC 32-bit data bus to a 68030 8 or 16-bit bus. Except DRAM and VGA controller, all peripherals work on this 68k-type bus. Full compatibility is therefore ensured with current acquisition boards and small peripherals.

16 and 8-bit Peripherals

The only 16-bit peripheral hooked on the bus is the acquisition board.
RETINE (A36) generates wait state timings and is used to switch between cold boot (return to default state) and warm boot (do a RESET, but keep current scope settings), and generates a bus error if max. access time is out and no peripheral has acknowledged the access.
ASSISE (A21) generates chip select signals for the bus sizer, BUDGET (A28) creates typical 68k signals (_BAS, _BDS, 16MHz clock).
The peripheral address decoding is done by a set of GALs (GRANDS (A20), PETITS (A29)) and a few multiplexers (A30, A22). GRANDS selects between main peripheral categories (VGA, DRAM, memory card, flash PROM, acquisition board or other peripherals), PETITS generates chip select signals for 8-bit peripherals (flash PROM, memory card, non-volatile RAM, Centronics and “others”). It also determines how many wait states are needed for peripherals not able to acknowledge a bus access. This is done by pulling low _DSACK0 after having sensed the corresponding number of wait states trough _BWT1 and _BWT3, which ends the current access.
The multiplexer A30 does a finer decoding between “others” decoded in PETITS, namely interrupt controller, small peripherals, serial interface, flash PROM chip 1 or 2, and status registers.

PCMCIA type I / II interface

This interface consists mainly of buffers for both data and address busses.
An OP amp (A10) and a MOS transistor (Q3) allow to switch off the memory card power supply while no card is plugged in, and turn it on slowly when plugged in.
The GAL CARDAN (A11) handles the card format and generates several control signals accordingly.
A16 (an hex D-type flip-flop) holds control bits for 12Vpp (flash programming voltage), DRAM memory mapping and memory card type. All bits of this register reset to zero when the _RESET signal goes active low, which means that their state is also guaranteed at power-up.
A9 and A12 are the read registers for several status bits.
Several EXOR gates (A17 and A18) invert the most significant address bits of the memory card whenever the SWAP jumper is plugged in, so that the first bytes are always located at 0xFFF00000, regardless of the size of the memory card. This allows to boot directly from a PCMCIA memory card.

Flash PROM

Two Intel 28F008-compatible 1MB PROMs (A24 and A25), are used.
From a hardware point of view, a flash PROM is the same as an EPROM in read mode. To write to it, however, a programming voltage (Vpp) needs to be applied to a pin. The 12V voltage is generated by a switching regulator (A26), controlled by a logic level (_EPPP).

NVRAM

This chip is powered through the lithium battery (VCT) when power is off. The chip select is held high through a pull-up resistor to VCT to avoid accidental overwriting while power is off.

Interrupt Controller

In order to keep compatibility with both 68k hardware and software, it is necessary to use a chip that prioritizes several interrupt sources. This is done by a NEC chip, an uPD71059. It scans eight interrupt pins and sends a unique interrupt to the processor when a (non-masked) interrupt appears.

Interrupt levels are assigned the following:

level 0	(lowest priority) acquisition board
level 1	small peripherals, unused
level 2	RS232
level 3	GPIB
level 4	small peripherals and acquisition board, unused
level 5	real time clock
level 6	time base (acquisition board)
level 7	(highest priority) only for test purposes. Linked to level 2 for debugging.

Floppy Controller

The floppy controller chip directly interfaces to a double or high-density disk drive. The floppy controller has a digital 8-bit input/output register, which is used to read several status lines from the drive (disk inserted, etc.).
In principle, the controller is able to provide an interrupt when accesses are completed. As these accesses are performed in non-time critical paths of the program, The interrupt line has been wired to the input register, so that the program has to poll this register until the interrupt line goes active.
The controller has it’s own timebase, a 24MHz crystal.

Centronics

Both external and internal Centronics ports are write-only. The data get latched in a 74HCT374 register (A45 for internal Centronics, A55 for external).

Small Peripheral Interface

This 8-bit interface is intended to allow external expansion to the processor board. A56 and A53 (74HCT541 tri-state buffers) buffer the address and control lines, and A62 (74HCT245, bi-directional tri-state buffers) buffer the data lines.
The address decoding is done on each peripheral board. The acknowledge for each access is also done by the peripheral device, so that there is no restriction on wait-states. The bus clock runs at 16mhz, and a reset line reinitializes the boards at the same time as the CPU.
Four interrupt lines are also included in this interface, so that interrupt-driven boards can be used (a good example is the 9300-4 GPIB/RS232 board, which uses interrupts 2 and 3).

Serial Interface for on-board Peripherals

Two GALs (SEVERE and SAVEUR) are used to access serial on-board devices, like the real time clock, option GAL, front panel and some parts of the acquisition board. The principle of such a serial access is the following:
every write or read to the serial interface allows to write or read one bit (the MSB of the byte). To write a byte to a serial device, you need eight accesses to the serial interface.
Many serial devices need the same protocol: you first send a command byte (read, write, clear, etc.), and then read or write one or several data (if required).
Depending on the address the serial interface is been accessed, the corresponding device gets selected (_SSER, _SFPR, _SLED or SRTC lines). A clock (_SCKA), a read data (SDRA or SDRD) and a write data (SDWA or SDWD) constitute the serial interface itself (the D suffix on read and write data lines means Digital, i.e. devices on the CPU board; an A suffix means devices on the Acquisition board).

RTC

The 68HC68T1 real time clock has several functions:

- keep a time-of-the-day and current-date information while the DSO is not powered on.
- generate a 32kHz clock for DRAM refreshment.
- generate a 128Hz periodic interrupt to force bus accesses from the processor (otherwise the watchdog timer would time out and reset the board) and allow periodic update of the time display (“scope alive”).

The chip uses it’s own 32.768kHz crystal to keep the time and derive all timings. A few discrete components around it leave the chip powered by the backup lithium battery while the rest of the board is not powered, and charge the battery when the power is on again.

Front Panel

The front panel LED can be controlled by a serial write access. The LED (write only) shares the same address as the option GAL (read only).
The LED is driven by the less significant bit (LSB) of the control register.

Watchdog and Reset Generation

The power supply is monitored by a TL7770-5 chip. Whenever the Vcc voltage goes below 4.8V (even for a short time !), a reset pulse is generated, whose width is determined by an RC time constant (33uF and internal resistor).
The second half of this chip serves as watchdog circuit. The processor needs to poll a sense line on that chip from time to time (typically a few ms). By doing this, a capacitor (33uF) is discharged. When not polled, it gets charged by a constant current, and when a given threshold is exceeded, a reset pulse is generated.
The LED connected goes off whenever the _RESET line is low, so a blinking LED indicates either no bus access for longer than a few hundreds of ms, or a problem (glitch) on the Vcc power supply.

Bus Error Generation

A bus error exception is generated when the _TEA pin is pulled low on the processor. The 603e expects a _TA signal as an acknowledge to the current data transaction, and inserts wait states as long as _TA has not been pulled low at the correct timing (refer to the MPC603e documentation for exact timing information's).
An external circuit is required to break the pending cycle if no device responds after a given time-out.
This is the job of the GAL RETINE (A36), which counts the number of wait states already passed (4 bit Gray counter). An external 4-bit counter (A59) extends the count to 160 (tbd) wait cycles before triggering a bus error.
An acknowledge (_DSACK1..0 lines) aborts the time-out count and finishes successfully the current cycle.

I/O Structure and GALs Involved

The following bloc diagram describes the peripheral decoding flow, and what GAL is involved in the decoding. The three frames group the peripherals into 8, 16 or 32-bit devices. The simple 3D-blocs represent an on-board device. The 3D-blocks with an arrow represent external devices (more generally: accessed through a connector).
GRANDS does the main decoding of peripherals and the 93xx-3 acquisition board.
PETITS does the sub-decoding for all 8-bit peripherals.
VIADUC handles the Motorola to Intel format decoding for the VGA controller.
CARDAN takes care of the PCMCIA interface timings.
PROFIL dispatches 8-bit data to the Centronics or the Floppy controller.
SAVEUR and SEVERE generate the serial clock and routes the data to the right serial device, including CLExxx, which is the option PAL.

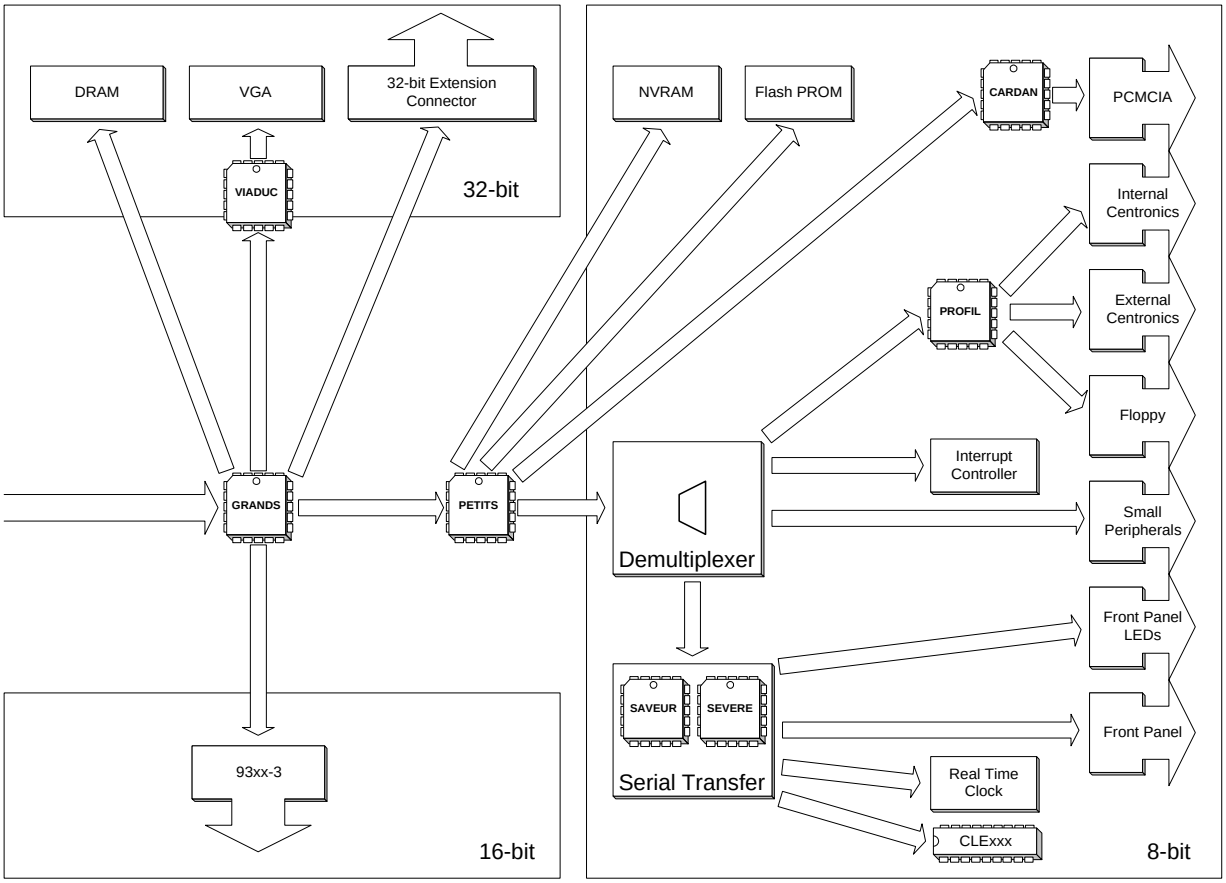


Fig 4-2: Peripheral Decoding and Data Bus Size

Not shown in Fig.4-2, are a few GALs for miscellaneous functions (like DRAM refreshing).
RASADE generates the RAS signals and the lower addresses for DRAM. It also supports the signals needed for interleaved burst mode.
OCCASE generates the CAS signals for DRAM.
RAMEUR is the main sequencer for the DRAM , and handles the access precharge and the refresh system.
BUDGET translates a 680x0 bus cycle into a PPC cycle, and handles fast cycles, like accesses to DRAM or VGA.
RETINE counts the wait states and generates a bus error if no response after too many (153) wait states. It also generates the system reset.
ASSISE decodes CPU space cycles and controls the bus sizer.

4.2 900079 Main Board

4.2.1 Introduction

The board is divided into five sections :

- Microprocessor control based on the MTC428 EPLD pair.
- Front-end based on the Hybrid HFE444 & HSY430 switchyard board to combine the input channel.
- Trigger based on the Hybrids HTR420 discriminator & MST429A smart trigger
- Analog Converter based on the HAM435 Sample&Hold and A/D converter and MNX427 min/max to pre-compute the data.
- Digital Acquisition based on the HMM434 Acquisition memory and SIMM DRAM module for buffer memory.
- Time base based on the MCG426 clock generator & MTB411A controller

4.2.2 Front End

The front-end system provides the signal conditioning for the ADC system.
All channel are identical, thus only one channel will be described here.

The main functions of the Front end without the amplifier (HFE444) are:

- Four channels operation, calibration with Software control
- Input protection (clamp + thermal detection) and coupling (AC, DC, 1 MΩ, 50 Ω).
- Attenuator by 10 in the 50Ω path and attenuator by 20 in 1MΩ path.
- Offset control and CAL control.

The main functions of HFE444 are:

- Amplitude normalization for the ADC system : at the BNC the dynamic range is 16 mV to 8V FS at 50Ω and to 16V FS (full scale) at 1 MOhm in a 1-2-5 step sequence and the ADC system input is 500 mV differential.
- Fine gain control to fill in the fixed vertical sensitivities.
- Bandwidth limit filter at 25 MHz and 200 MHz.

Power off State : 1 MΩ input

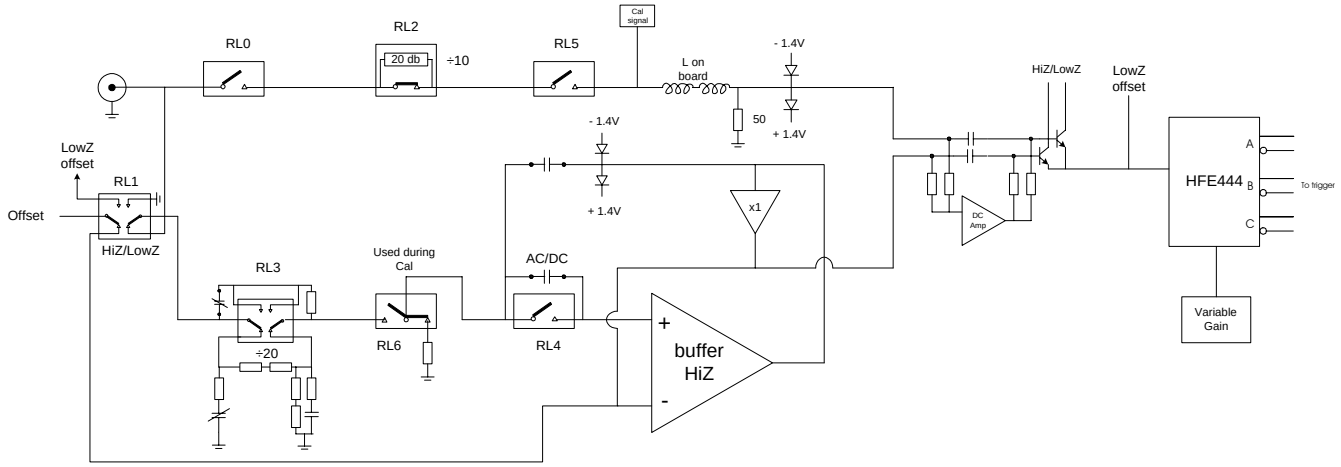


Fig 4-3: Front End Power off State

- Relay RL1 selects the input and offset voltage between the Hi-Z (1 MΩ) and the 50Ω path.
- The 50Ω path is then disconnected by RL0 and the signal will be in the 1 Mohm input.
- Relay RL2 selects the input between divide-by-10 or direct for the signal in the 50Ω path.
- Relay RL3 selects the input between direct or divide-by-20 for the signal in the HiZ path.
- Relay RL4 sets the AC/DC coupling in HiZ.
- Relay RL5 is only used during calibration.
- Relay RL6 clamps the HiZ amplifier when not selected..
- Bias_HiZ and Bias_LoZ is used to bias transistors Qx003 and Qx004 to select between the HiZ path or LowZ path as input to the HFE through the DC amplifier.
- There is no AC/DC coupling in the 50Ω path.

50Ω input : Direct Path

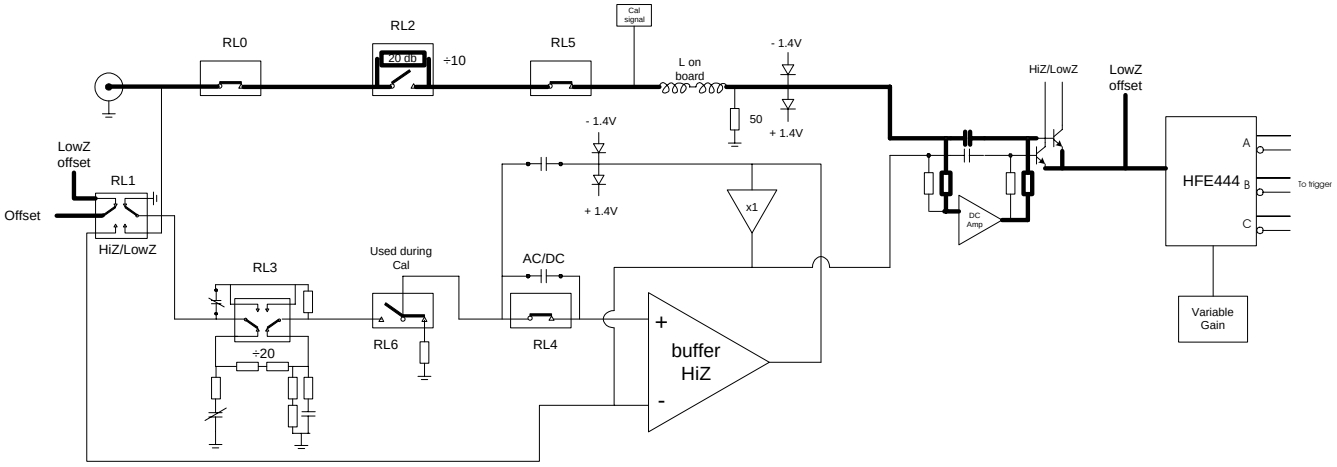


Fig 4-4: 50Ω input direct path

50Ω input : Divide-by-10 Path

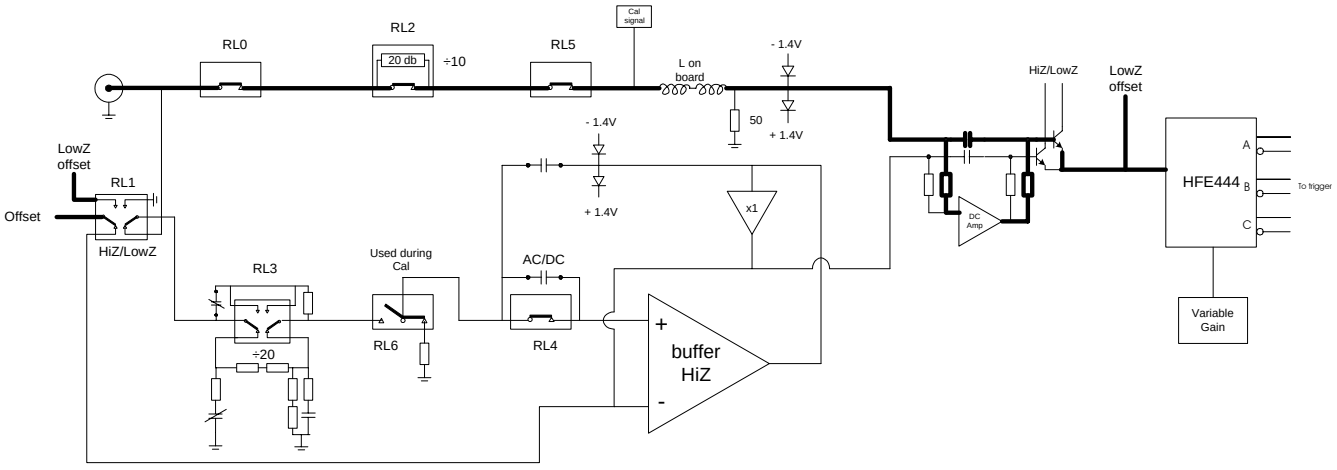


Fig 4-5: 50Ω divide by 10 path

1MΩ input : Direct Path

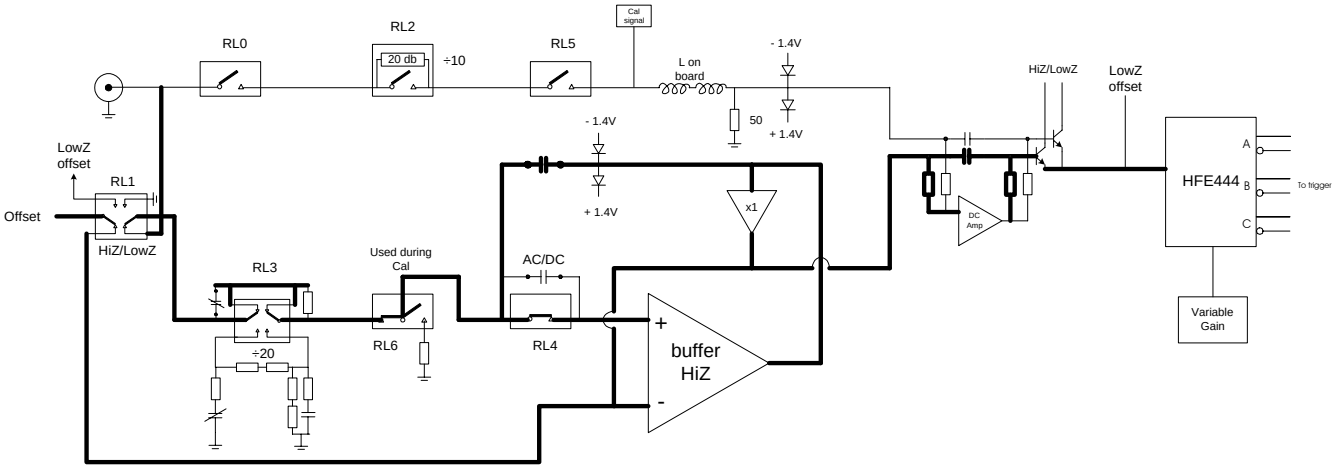


Fig 4-6: 1MΩ direct path

1MΩ divide by 10 AC coupled path

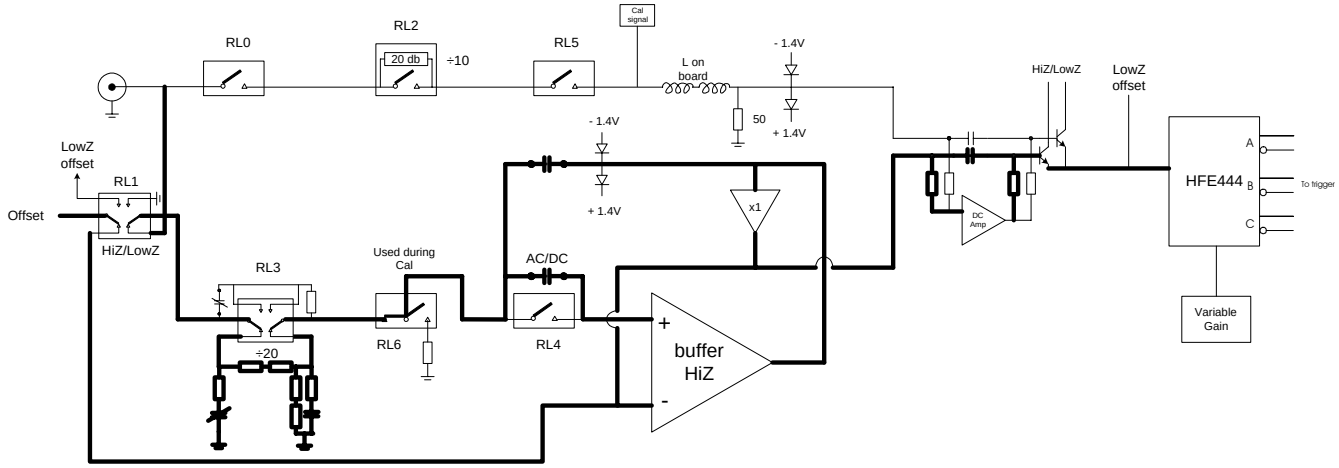


Fig 4-7: 1MΩ divide by 10 AC coupled path

Front End Analog controls

- One precision DAC with an associate circular memory (μP system) drives and refreshes a multiple sample-and-hold system. The DC calibration control is common to all four channels. Each channel has two analog controls.

4.2.3 900079 Acquisition Block Diagram

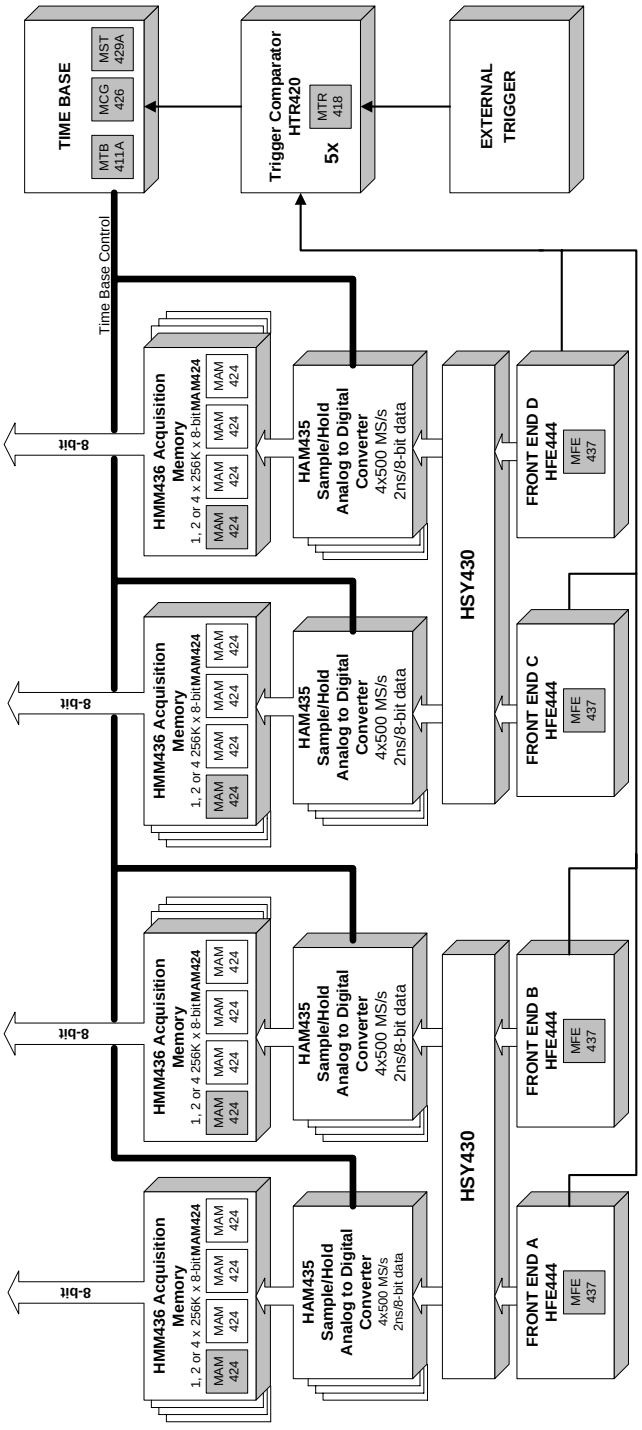


Fig 4.8: Front End, Trigger, Sample&Hold, Analog to Digital, Memory

4.2.4 Two and Four Channel mode

Four channel mode

- All BNC inputs are active

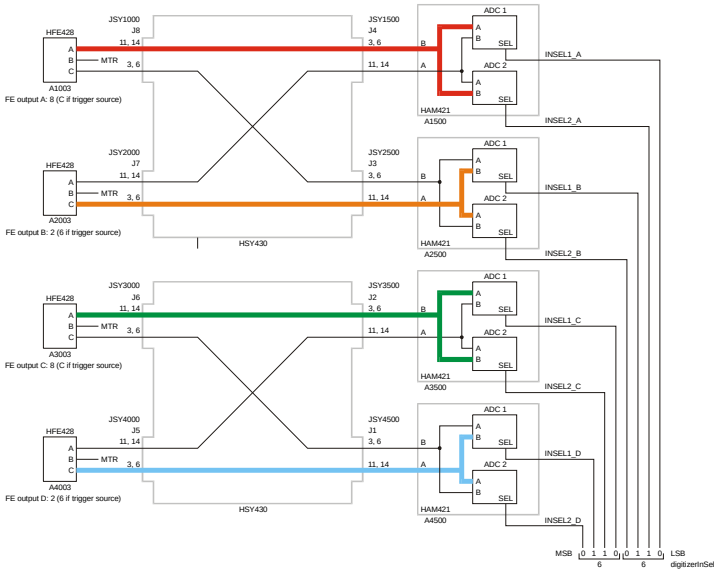


Figure 4-9 Four Channel Mode Signal Routing

Two channel mode

- Two channel mode, BNC inputs for channel 2 and 3 are active, ADC's for channel 1 & 2 are used for signal on channel 2 input, ADC's for channel 3& 4 are used for signal on channel 3 input.

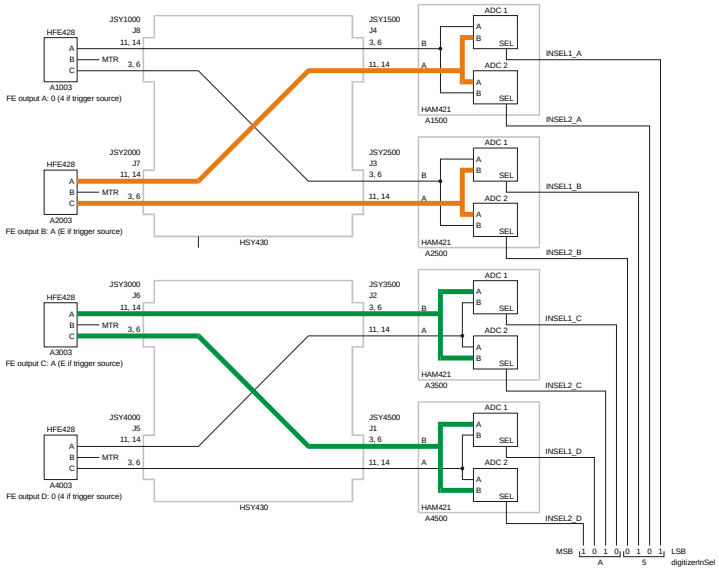


Figure 4-10 One and Two Channel Mode Signal Routing

4.2.5 900079 Control & Transfer Block Diagram

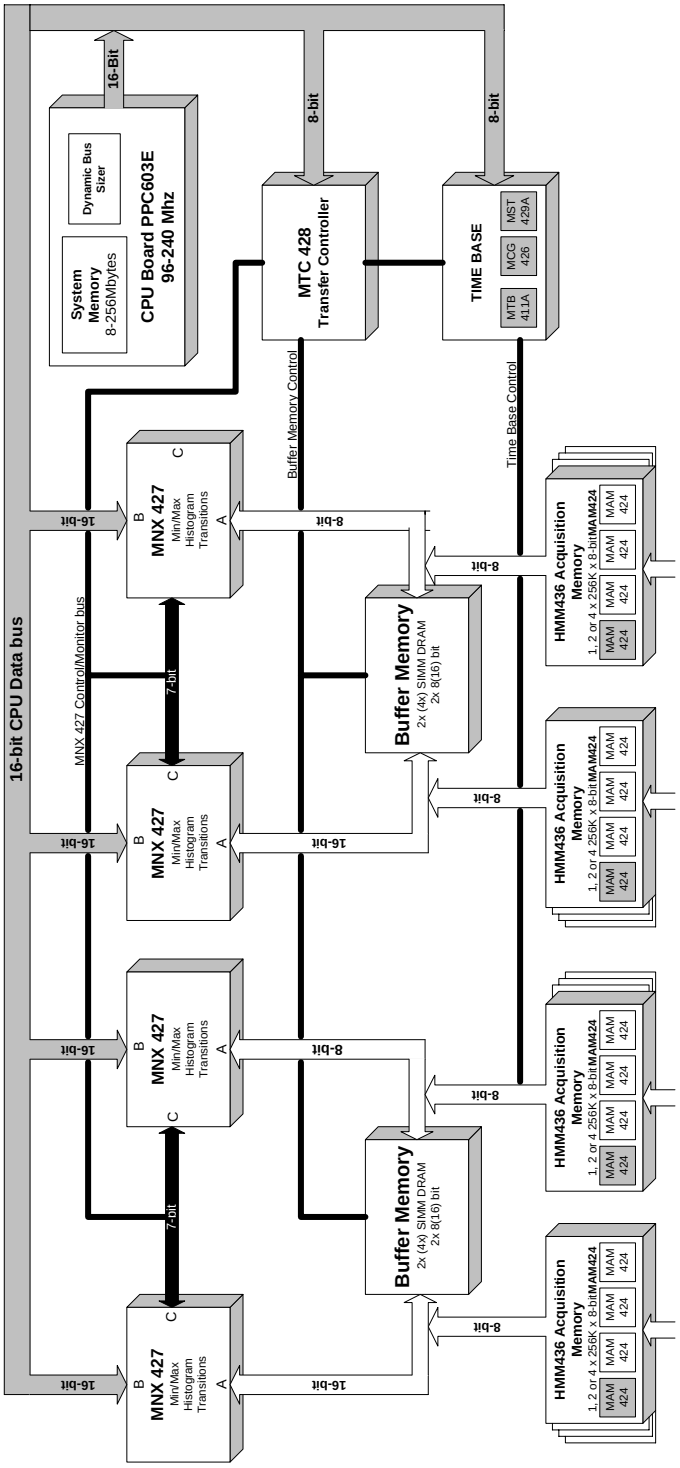


Fig 4.11: Processor Control, Min/Max, Buffer Memory, Transfer

4.2.6 Trigger

The different trigger couplings are :

- DC
- AC : cut off frequency is almost 10 Hz.
- LF REJ : single pole high pass filter with a cut off frequency at 50 kHz.
- HF REJ : single pole low pass filter with a cut off frequency at 50 kHz.
- TBWL : single pole low pass filter at 25 MHz.

Analog Controls

A sample and hold fed by the precision DAC provides the threshold level.
The addresses are :

TV Trigger

Each channel has a pick-off after the HFE428 or after the high impedance buffer for external trigger. The TV trigger source is selected via bit TVS and drives a times 10 amplifier with complementary outputs. These outputs are selected (_TVINV) depending on the state of the selected HFE428 gain.
The TV trigger uses a commercial chip (LM1881) and provides two outputs, TV1 & TV2. This circuit is able to trigger on different TV line number standards.

4.2.7 Analog to Digital Converter

Introduction

The analog to digital converter system does the signal conversion to 8 bits, using the following circuits:

- **HAM435**: Hybrid Acquisition Module, Sample&Hold plus ADC

  MSH437: Monolithic Sample and Hold. performs the track&hold before the ADC.

  MAD422: Analog to Digital converter, maximum clock speed of 500 Ms/s

- **HMM436**: Hybrid Memory module, up to 4 Mbytes per Channel

  MAM 424: Monolithic Access Memory

- **MNX427**: Monolithic MIN-MAX

- **Buffer Memory** : 16Mbytes

- **HSY430**: Interleaving Channel

4.2.8 Time Base

Introduction

The time base includes three circuits:

- **MCG426**: generates sampling clocks: 12.5 MHz up to 2GHz
  generates clocks for the MTB411
  interleaves sampling clocks to increase sampling rate and memory depth.

- **MTB411A**: Time Base System
  TDC interpolator and Real Time computation
  Trigger circuitry
  Frequency divider

- **MST429A**: Single source trigger, Standard trigger, Hold off, Pulse width & interval
  Multiple source trigger, State qualified, Edge qualified

Block Diagram

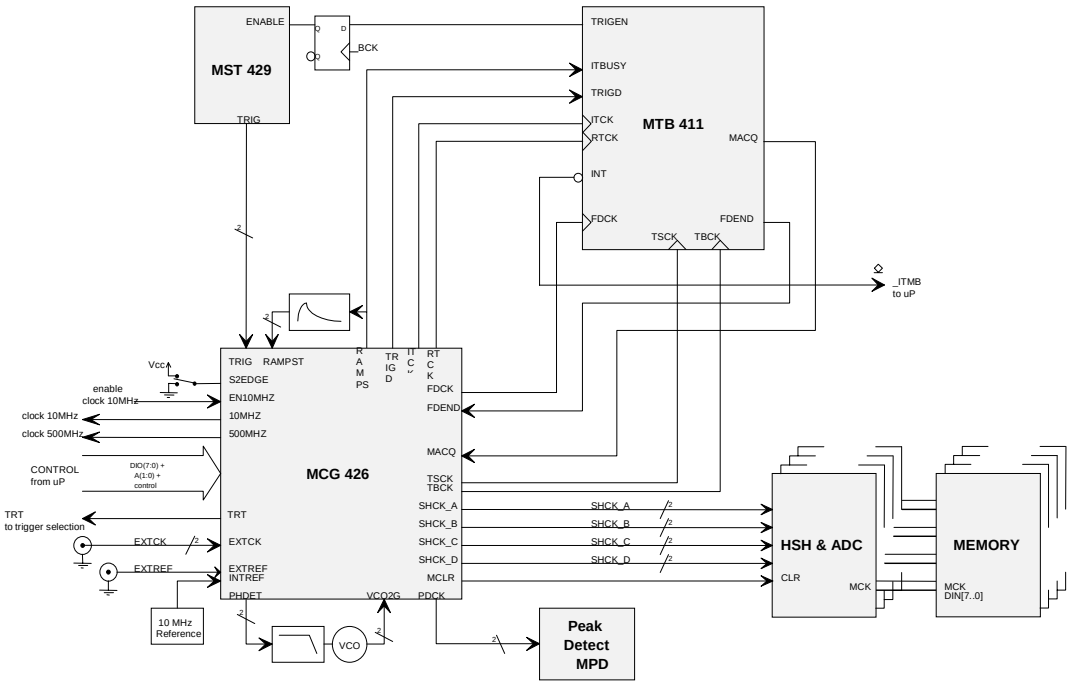


Fig 4.12: Time Base Block Diagram

4.3 F9301-4 GPIB and RS 232 Interface

4.3.1 Block Diagram

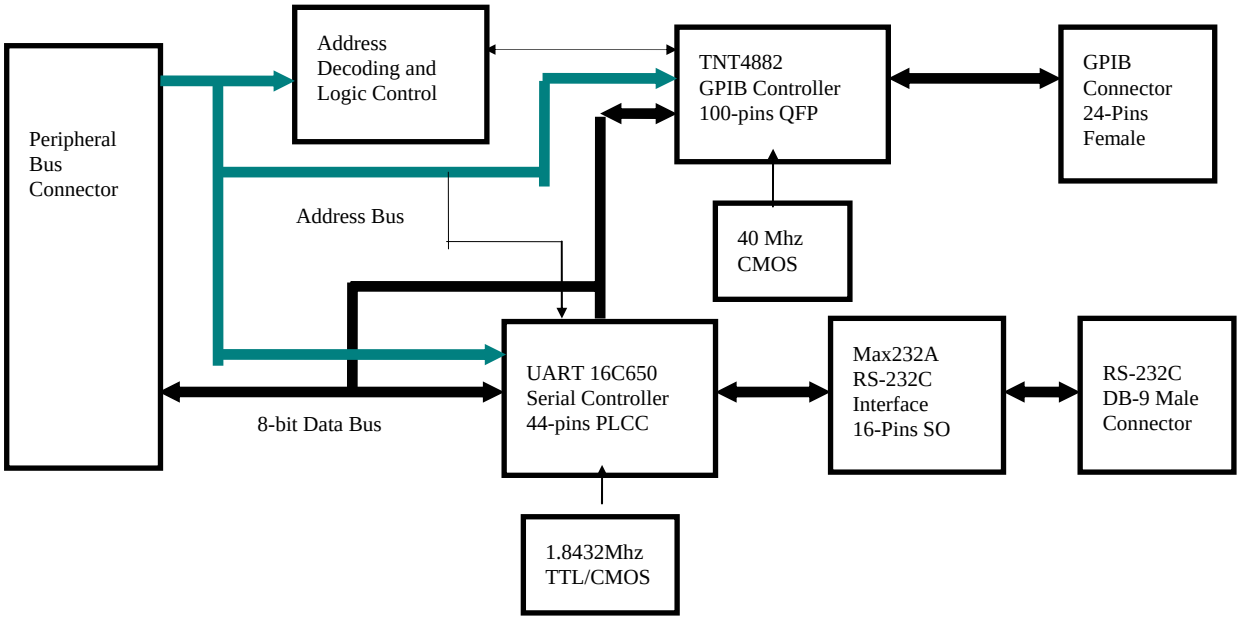


Fig 4.13: GPIB & RS232 Interface Block Diagram

This board is connected to the processor through a flat cable.
Data bus is 8 bits, address bus: 12 bits.
Address 0180 000 to 0180 00FF.

4.3.2 F9301-4 RS 232 Serial Interface

Based on the ST16650 from EXAR or Startech.

- Clock frequency 1.8432 MHz.
- RTC/CTS signals are connected
- DCD input is biased and the DTR output is not wired
- Asynchronous communication up to 1Mbits/sec
- 32 bytes receive and transmit FIFOs buffer
- Connector compatible with a DB9-P (9 pin male).

4.3.3 F9301-4 GPIB Interface

Based on the circuit TNT4882 from National Instruments.

- Clock frequency 40 MHz.
- Up to 1.5 Mbytes/sec using interlocked IEEE 488.1 handshake
- Two 8-bit 16-deep FIFOs buffer data between GPIB and CPU

The GPIB address is set by software and stored in non-volatile memory.

4.4 LCDFP9615 Front Panel

The front panel assy is connected to the processor board with a flat cable. Power supply and control signals are supplied from the processor. The front panel is divided into several sections:

- Display using 10.4inch TFT color LCD Module
- F9601-61 Floppy disk drive assy
- S9615-21 Buffer board which interfaces the digital signals from the processor to the TFT display unit
- S9615-52 board with Motorola 68HC05C4 processor, encoders, and serial data interface.
- F9615-5 matrix keypad with push buttons.

4.5 F9300-7 Printer Controller Option

- Based on the Internal graphic printer LPT5446, and LPT5000 series control chip set from Seiko instrument Inc (Technical reference 39019-2234-01)
- PT501P01 CPU
- PT500GA1 Gate array
- Address 0130 0100
- Interrupt level 2

4.6 PS9611 Power Supply

The PS9611 is a nine output 300 W AC-DC switching mode power supply.

4.6.1 Specifications

AC Input Voltage

85-132VAC and 170-264VAC, auto-ranging universal input, provides automatic sensing of 115 or 230VAC input voltage. Power factor correction for compliance with EN61000-3-2: 1995 standard (harmonic current emissions) under all conditions of input voltage, input frequency, loads and temperature ranges.
AC power enters the DSO chassis thru an IEC320 input receptacle, fuses and an EMI line filter. The filter high frequency noise generated by the DSO from getting out on to the AC line.

Input Frequency: AC input Frequency range of 47 Hz to 63 Hz.

Inrush Current: less than 30 A over full line voltage ranges and input frequency

DC Output Specifications

Output	Adjustment Range	Nominal Load	Maximum Load
+5 (1)	+4.8 to +5.4V	15A	20A
+3 (1)	+2.9 to +3.5V	10A	20A
-2 (1)	-1.9 to –2.6V	5A	15A
-5 (1)	-4.8 to -5.4V	15A	20A
+6 (1)	+5.6 to +6.2V	2.5A	4A
-6 (1)	-5.6 to -6.2V	2.5A	4A
+15	+14.8 to +15.4V	2.5A	4A
-15	-14.8 to -15.4V	2A	3A / 8A
-12	-11.5 to -14.0V	0.5A	1A

Note:(1) with remote sense.

Output power: 300W

Ripple and Noise: less than 25 mV

Hold up Time: 25 mV at full load

Transient response: recovery time <1.2 msec to within 50 mV of its final value

Protections: over current, over voltage, over temperature

Cooling: PS9611 is cooled by a forced airflow provided by a fan that is integrated inside the unit.

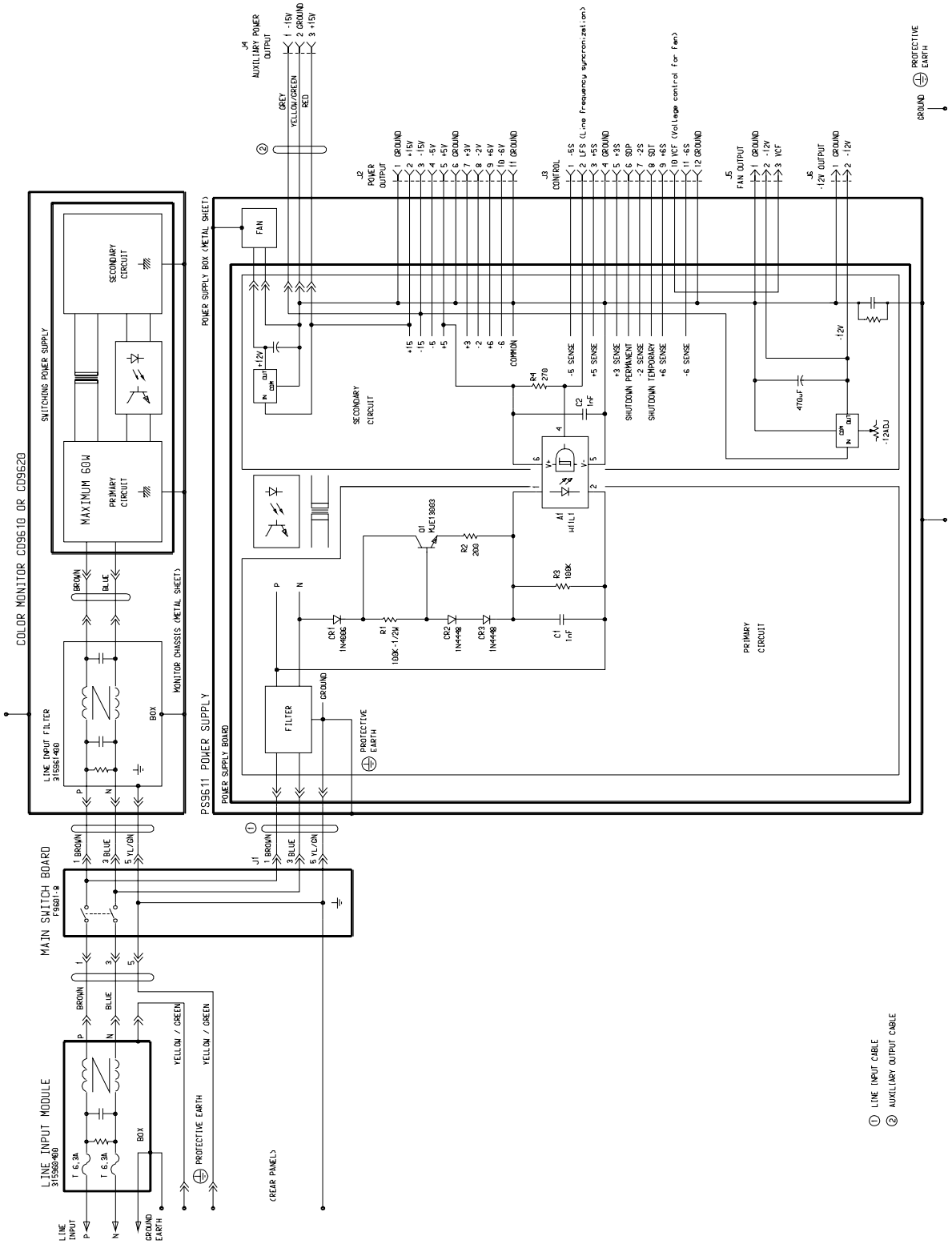
Environmental: Operating temperature range 0 °C to + 55 °C
Storage temperature range - 55 °C to + 85 °C
Operating humidity from 5% to 95% RH.
Operating Altitude (max) 5000m or 15000 feet

Safety Standards: CE, UL, CSA, TUV
EN61010-1:1993 (IEC1010-1:1995), UL3111-1,
CSA-C22.2 No.61010-1.
Protection class I, pollution degree 2, installation category II.

EMI: EN50081-1:1992, EN55022:1987 Class B, EN61000-3-2&3:1995 Class D

Immunity: EN50082-1:1994, EN61000-4-2,4,5,8&11:1995,
IEC1000-4-2,3,4,5,6,8&11

4.6.2 Power Supply Block Diagram



5. Performance Verification

5.1 Introduction

This chapter contains procedures suitable for determining if the LC564DL Digital Storage Oscilloscope performs correctly and as warranted.
They check all the characteristics listed in subsection 5.1.1.

Because they require time and suitable test equipment, you may not need to perform all of these procedures, depending on what you want to accomplish.

In the absence of the computer automated calibration system based on LeCroy Calibration Software (LeCalsoft), this manual performance verification procedure can be followed to establish a traceable calibration.
It is the calibrating entities' responsibility to ensure that all laboratory standards used to perform this procedure are operating within their specifications and traceable to required standards if a traceable calibration certificate is to be issued for the LC564DL Digital Storage Oscilloscope.

5.1.1 List of Tested Characteristics

This subsection lists the characteristics that are tested in terms of quantifiable performance limits.

- Input Impedance
- Leakage Current
- Peak to Peak and RMS Average noise level
- Positive and Negative DC linearity
- Positive and Negative Offset
- Bandwidth
- Trigger Level
- Smart Trigger
- Time Base Accuracy
- Rise Time

5.1.2 Calibration Cycle

The LC564DL Digital Storage Oscilloscope requires periodic verification of performance. Under normal use (2,000 hours of use per year) and environmental conditions, this instrument should be calibrated once a year.

5.2 Test Equipment Required

These procedures use external, traceable signal generators, DC precision power supply, step generator and digital multimeter, to directly check specifications.

Instrument	Specifications	Recommended
Signal Generator Radio Frequency	Frequency : .5 MHz to 1 GHz Frequency Accuracy : 1 PPM	HP8648B or equivalent
Signal Generator Audio Frequency	Frequency : 0 to 5 kHz Amplitude : 8 V peak to peak	LeCroy LW420 or HP33120A or equivalent
Voltage Generator DC Power Supply	Range of 0 to 20 V, in steps of no more than 15 mV	HP6633A or equivalent
Step Generator Fast Pulser	Rise time 350ps ± 100 ps Overshoot 3.5 % ± 1 %	LeCroy 4969A + PB049 or equivalent
Power Meter + Sensor	Accuracy ±1 %	HP437B + 8482A or equivalent
Digital Multimeter Volt & Ohm	Voltmeter Accuracy : 0.1 % Ohmmeter Accuracy : 0.1 %	Keithley 2000 or equivalent
Adapter	50Ω to 1MΩ	LeCroy 4962-10
Coaxial Cable, 1 ns	50Ω, BNC, length 20 cm,	LeCroy 480232001
Coaxial Cable, 5 ns	50Ω, BNC, length 100 cm,	LeCroy 480020101
2 Attenuators, 20 dB	50Ω, BNC, 1 % accuracy	LeCroy 402200402
Attenuator, 6 dB	50Ω, BNC, 1 % accuracy	LeCroy 402600403
Terminator, 2 W	50Ω, BNC, Feed-Through	LeCroy 402323001
T adapter	50Ω, BNC T adapter	LeCroy 402222002

Table 5-1 : Test Equipment

5.2.1 Test Records

The last pages of this document contain LC564DL test records in the format tables. Keep them as masters and use a photocopy for each calibration.

5.3 Turn On

If you are not familiar with operating the LC564DL, read the operator's manual.

- Switch on the power using the power switch.
- Wait for about 20 minutes for the scope to reach a stable operating temperature, and verify:

  - the display turns on after about 10 seconds and is stable.
  - the range of intensity and grid intensity is reasonable.

5.4 Input Impedance

Specifications

DC 1.00 MΩ ±1 %
AC 1.027 MΩ ±2 %
DC 50Ω ±1.25 %
EXT DC 50Ω ±3%
EXT DC 1.00 MΩ ±2%

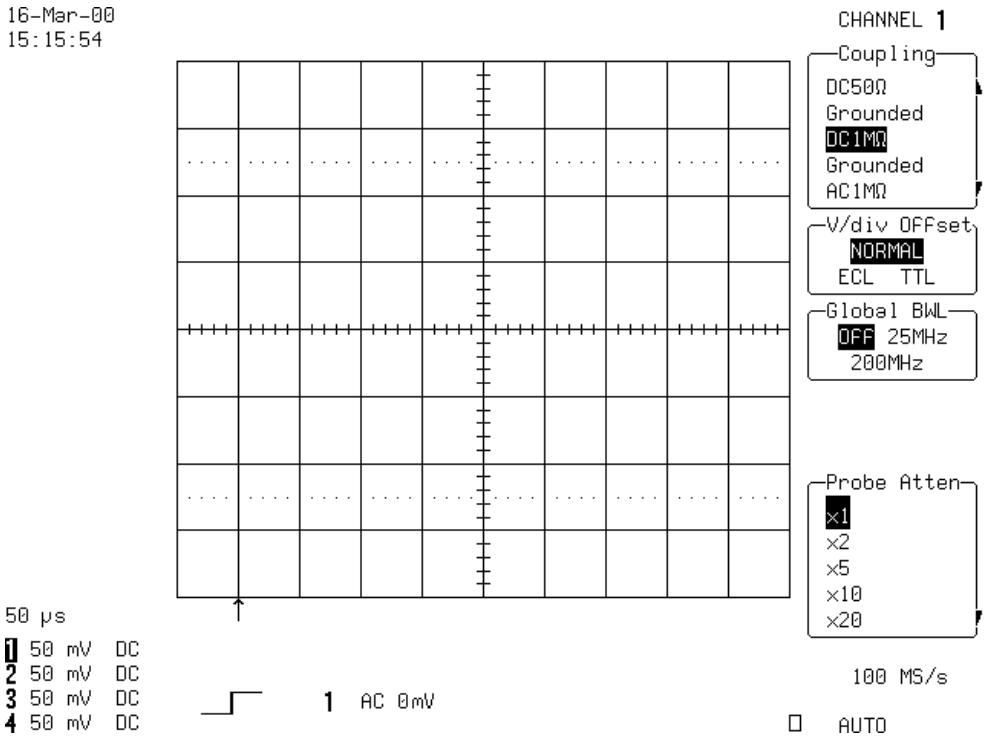
The impedance values for 50Ω, 1MΩ and Gnd couplings are measured with a high precision digital multimeter. The DMM is connected to the DSO in 4-wire configuration (input and sense), allowing for accurate measurements.

5.4.1 Channel Input Impedance

a. DC 1MΩ

- Recall **LC564D001.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	**50 mV/div.** on all 4 Channels
Time base	:	**50 µsec/div.**
Trigger mode	:	**Auto**

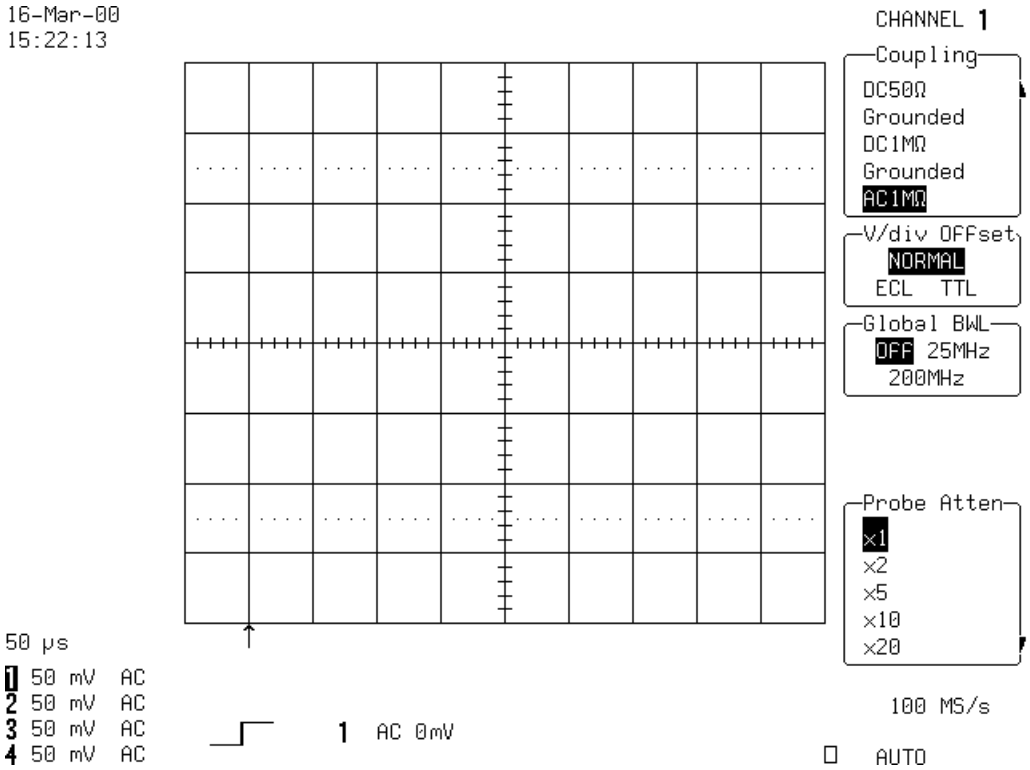


- Set the DMM with **Ohms and Ohms sense** to provide a 4 wire measurement.
- Connect it to Channel 1.
- Measure the **input impedance**. Record it in Table 2, and compare it to the limits.
- Repeat the above test for all input channels.
- Recall **LC564D002.PNL** or Set Input gain to **200 mV/div.** on all 4 Channels
- Repeat the test for all input channels.
- Record the measurements in Table 2, and compare the test results to the limits in the test record.

b. AC 1MΩ

- Recall **LC564D003.PNL** or configure the DSO as shown in 5.4.1.a, and for each Channel make the following change :

  Input Coupling : **AC 1MΩ**
- For all input channels measure the **input impedance**.



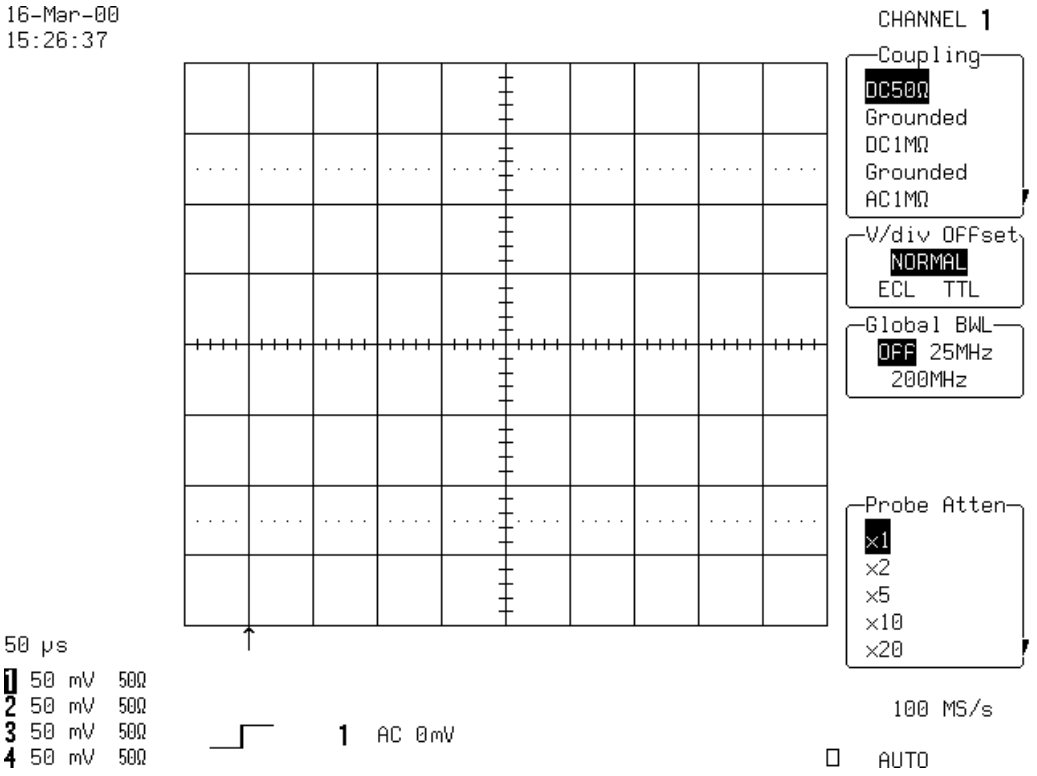
- Record the input impedance in Table 2, and compare it to the limits.

- Recall **LC564D004.PNL** or Set Input gain to **200 mV/div** on all 4 Channels.
- Repeat the test for all input channels.
- Record the measurements in Table 2, and compare the results to the limits in the test record.

c. DC 50Ω

- Recall **LC564D005.PNL** or configure the DSO as shown in 5.4.1.a, and for each Channel make the following change:

Input Coupling : **DC 50Ω**



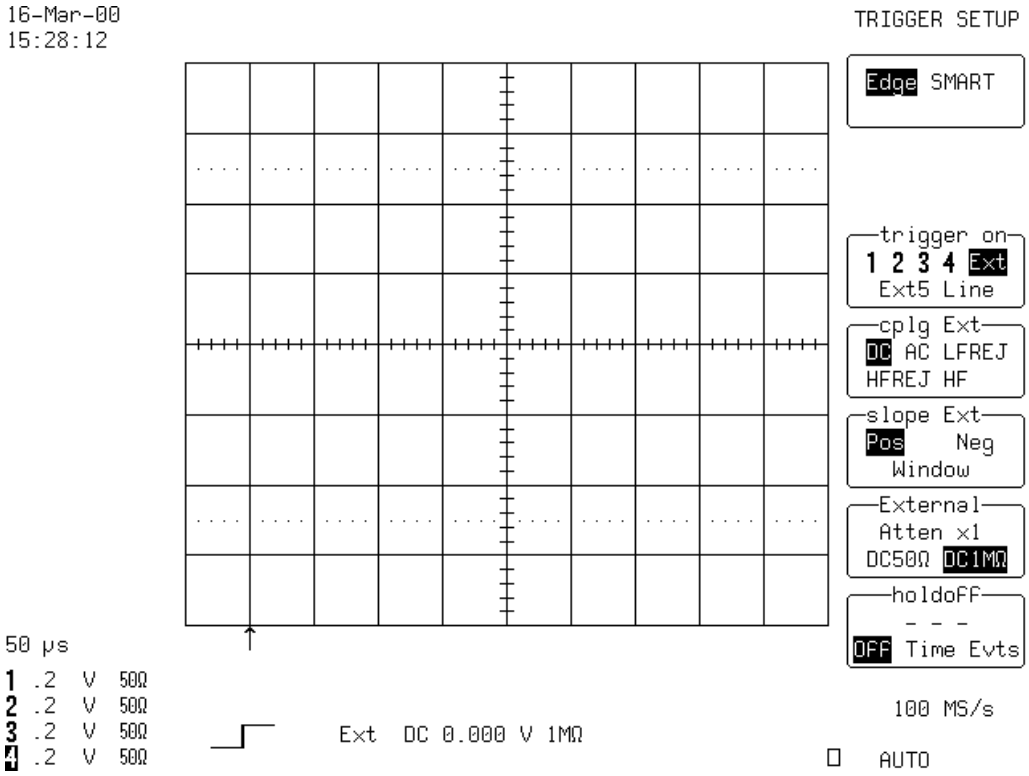
- For all input Channels, measure the input impedance.
- Record the **input impedance** in Table 2, and compare it to the limits.
- Recall **LC564D006.PNL** or set Input gain to **200 mV/div.** on all 4 Channels
- Repeat the test for all input channels. Record the measurements in Table 2, and compare the results to the limits in the test record.

5.4.2 External Trigger Input Impedance

a. DC 1MΩ

- Recall **LC564D007.PNL** or configure the DSO :

Trigger mode	:	**Auto**
Select Setup trigger		
Trigger on	:	**EXT**
Cplg Ext	:	**DC**
External	:	**DC 1MΩ**
Time base	:	**50 µsec/div.**



- Connect the DMM to External, and measure the input impedance.
- Record the input impedance in Table 2, and compare it to the limits.
- Recall **LC564D008.PNL** or set trigger to Ext/5
- Measure the **input impedance**.
- Record the test result in Table 2, and compare the result to the limits in the test record.

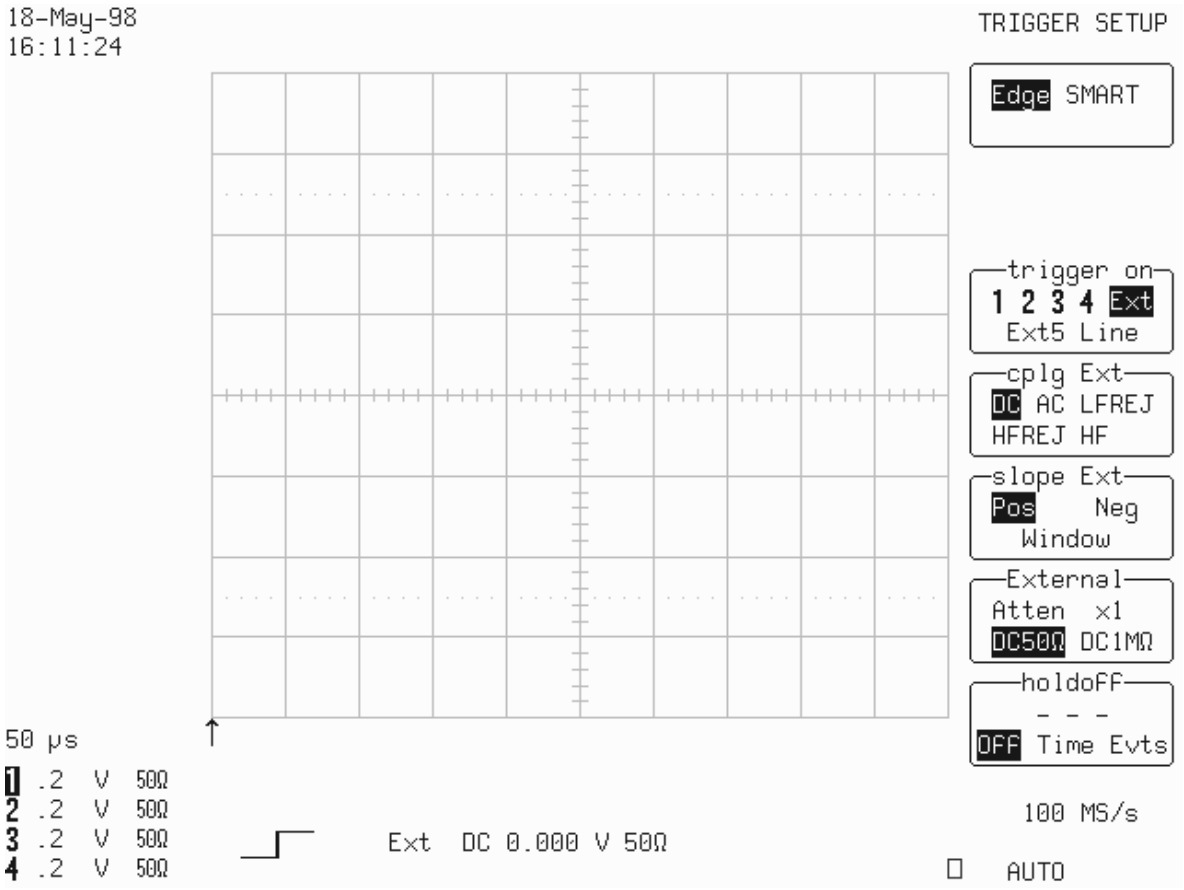
b. DC 50Ω

- Recall **LC564D009.PNL** or configure the DSO :

  Select Setup trigger

  Trigger on : **EXT**

  External : **DC 50Ω**



- Connect the DMM to External, and measure the **input impedance**.
- Record the input impedance in Table 2, and compare the result to the limit in the test record.
- Recall **LC564D010.PNL** or configure the DSO:

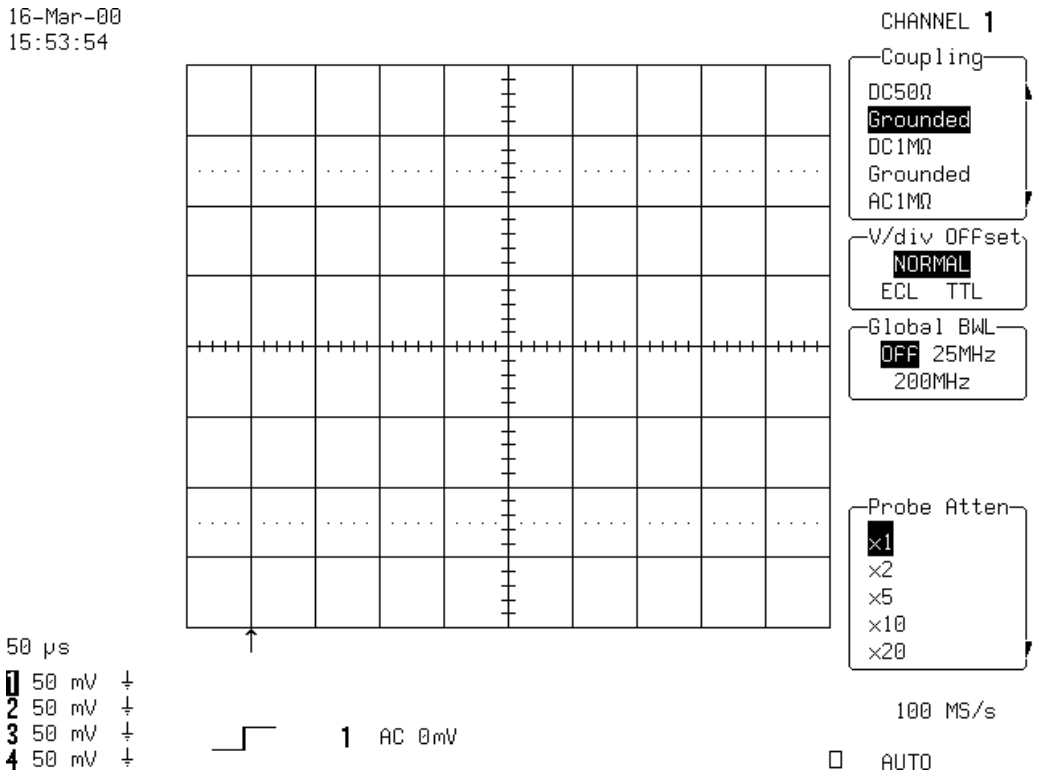
  Trigger on : EXT/5

- Measure the **input impedance**.
- Record the input impedance in Table 2, and compare the result to the limit in the test record.

5.4.3 Ground

- Recall **LC564D011.PNL** or configure the DSO as shown in 5.4.1.a, and for each Channel make the following changes :

  Input Coupling : **Grounded**



- Connect the DMM to Channel 1, and measure the **input impedance.**
- Record the input impedance in Table 2, and compare the result to the limit in the test record.
- Repeat the test for all input channels.
- Record the measurements in Table 2, and compare the results to the limits in the test record.

5.5 Leakage Current

Specifications

DC 1MΩ, AC 1MΩ, DC 50Ω, EXT DC 50Ω : ±1 mV
EXT DC1MΩ : ±2 mV

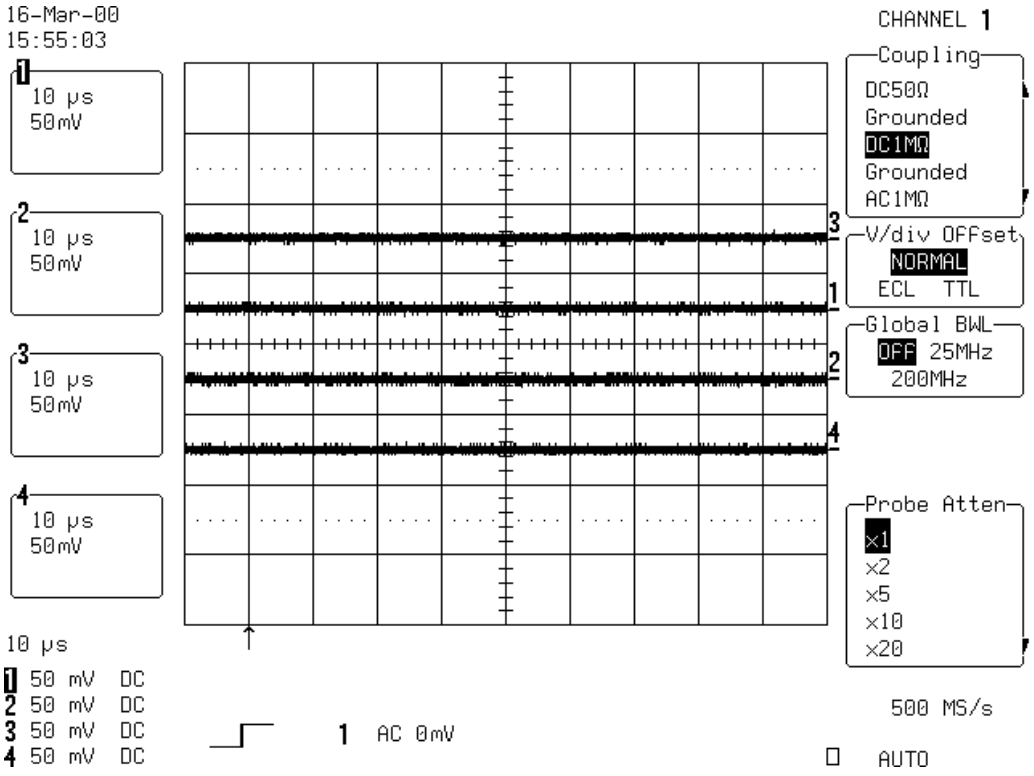
The leakage current is tested by measuring the voltage across the input channel.

5.5.1 Channel Leakage Current

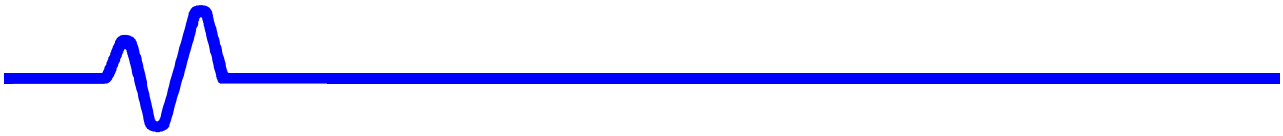
a. DC 1MΩ

- Recall **LC564D012.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	**50 mV/div.** on all 4 Channels
Trigger mode	:	**Auto**
Time base	:	**10 µsec/div.**



- Set the DMM to measure Volts, and connect it to Channel 1.



- Measure the **voltage** and enter it in Table 3. Compare it to the limits.
- Repeat the test for all input channels.
- Recall **LC564D013.PNL** or set Input gain to **200 mV/div.** on all 4 Channels
- Repeat the test for all input channels. Record the measurements in Table 3, and compare the results to the limits in the test record.

b. DC 50Ω

- Recall **LC564D014.PNL** or configure the DSO as shown in 5.5.1.a and for each Channel make the following changes :

  Set Input Coupling : **DC 50Ω**

- Connect the DMM to Channel 1.
- Measure the **voltage** and enter it in Table 3. Compare it to the limits.
- Recall **LC564D015.PNL** or set Input gain to **200 mV/div.** on all 4 Channels
- Repeat the test for all input channels.
- Record the measurements in Table 3, and compare the results to the limits in the test record.

5.5.2 External Trigger Leakage Current

a. DC 50Ω

- Recall **LC564D016.PNL** or configure the DSO as shown in 5.5.1.a and make the following changes :

  Select Setup trigger
  Set Trigger on : **EXT**

  External : **DC 50Ω**

- Connect the DMM to External.
- Measure the **voltage** and enter it in Table 3. Compare it to the limits.

b. DC 50Ω EXT/5

- Recall **LC564D017.PNL** or configure the DSO as shown in 5.5.1.a and make the following changes :

  Select Setup trigger
  Set Trigger on : **EXT/5**

  External : **DC 50Ω**

- Connect the DMM to External.

- Measure the **voltage** and enter it in Table 3. Compare it to the limits.

5.6 Average Noise Level

Description

Noise tests with open inputs are executed on all channels for both 1MΩ and 50Ω input impedance, with AC and DC input coupling, 0 mV offset, at a gain setting of 10 mV/div., and different Time base settings.
The scope parameters functions are used to measure the Peak and RMS amplitude

5.6.1 Peak to Peak Noise

Specifications

9 % of full scale or 7.2 mV Peak-Peak at 10 mV/div.

a. DC 1MΩ

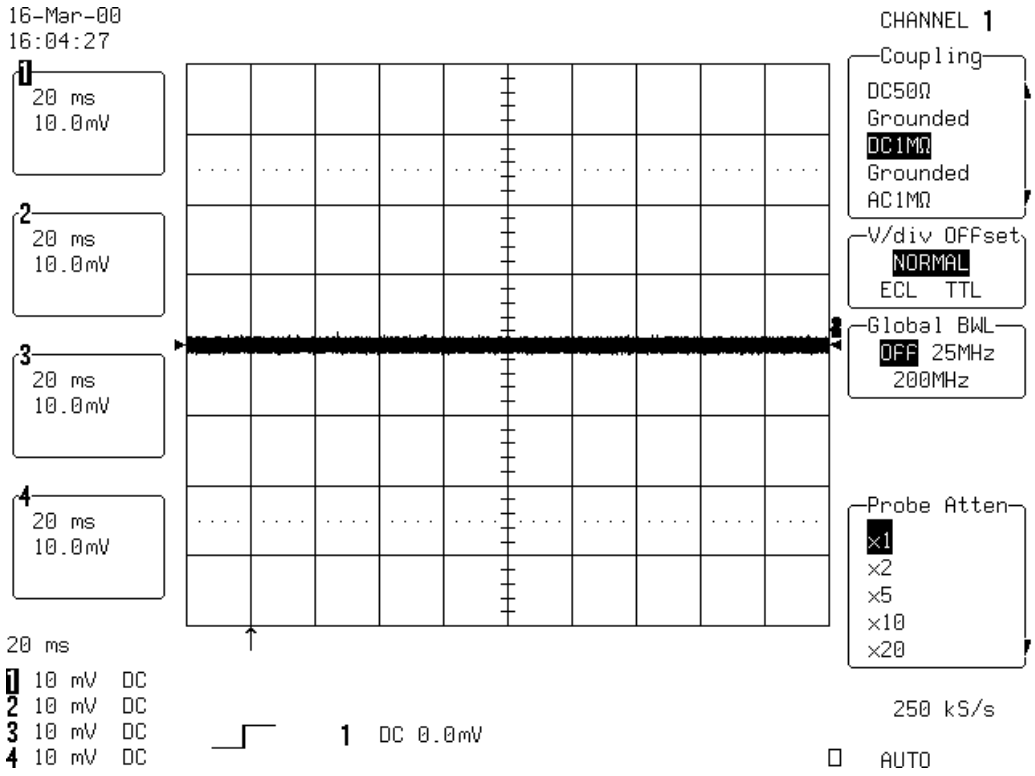
With no signal connected to the inputs

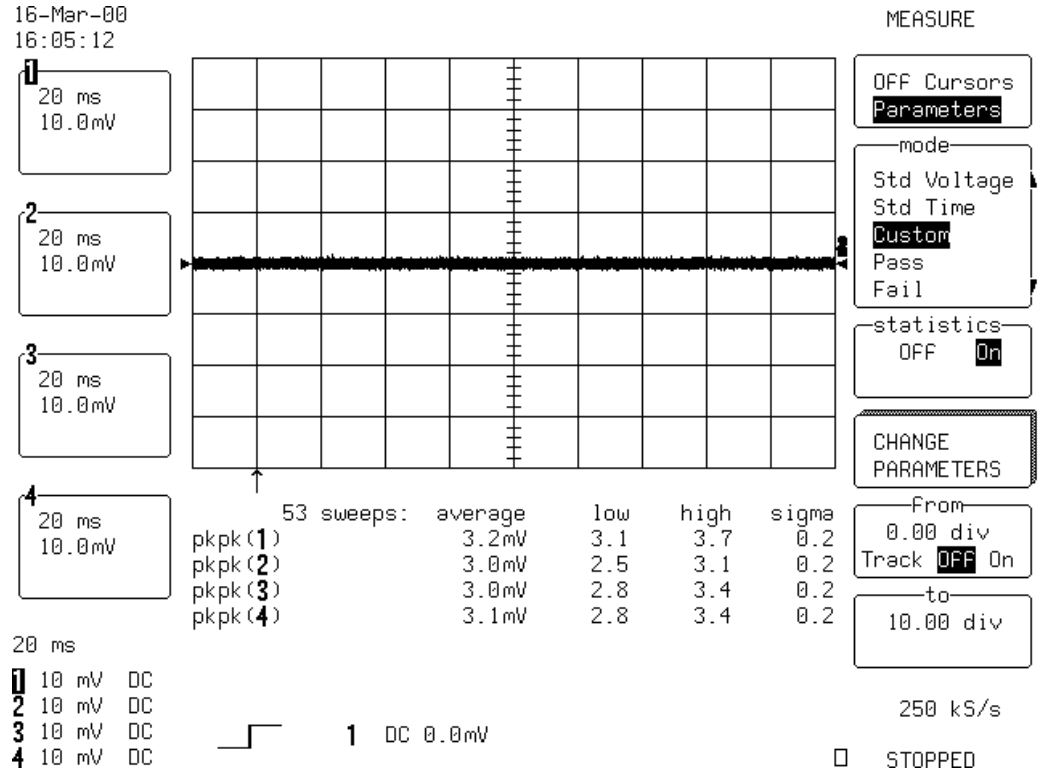
- Recall **LC564D018.PNL** or configure the DSO :

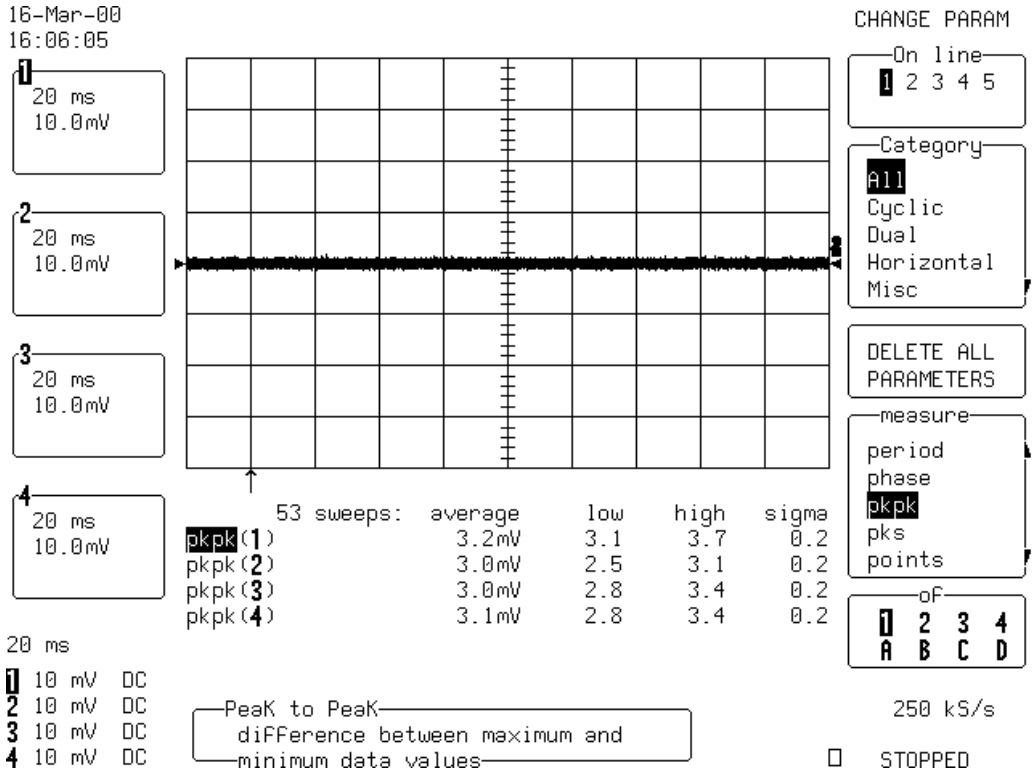
  Panel Setups : **Recall FROM DEFAULT SETUP**
  Channels Trace ON **Channel 1, Channel 2, Channel 3 & Channel 4**
  Input Coupling : **DC 1MΩ** on all 4 Channels
  Input gain : **10 mV/div.** on all 4 Channels
  Input offset : **0.0 mV** on all 4 Channels
  Trigger setup : **Edge**
  Trigger on : **1**
  Coupling 1 : **DC**
  Trigger Mode : **Auto**

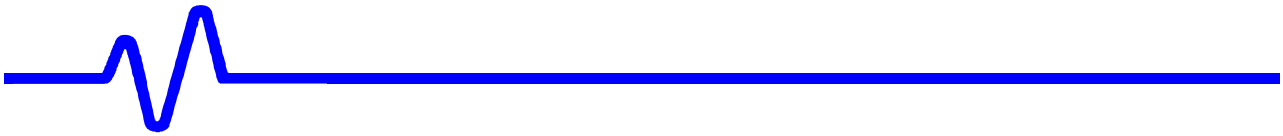
  Time base : **20 msec/div.**
  Channel use : **4**

Record up to	:	**50 k Samples**
Press	:	**Cursors/Measure**
Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**On**
Change parameters		
Category	:	**All**
On line 1	:	**Measure pkpk of Ch1**
On line 2	:	**Measure pkpk of Ch2**
On line 3	:	**Measure pkpk of Ch3**
On line 4	:	**Measure pkpk of Ch4**
On line 5	:	**no parameter selected for line 5**




16-Mar-00
16:05:12
MEASURE
1 20 ms 10.0mV
2 20 ms 10.0mV
3 20 ms 10.0mV
4 20 ms 10.0mV
OFF Cursors
Parameters
mode
Std Voltage
Std Time
Custom
Pass
Fail
statistics
OFF On
CHANGE PARAMETERS
From
0.00 div
Track OFF On
to
10.00 div
53 sweeps: average low high sigma
pkpk(1) 3.2mV 3.1 3.7 0.2
pkpk(2) 3.0mV 2.5 3.1 0.2
pkpk(3) 3.0mV 2.8 3.4 0.2
pkpk(4) 3.1mV 2.8 3.4 0.2
20 ms
1 10 mV DC
2 10 mV DC
3 10 mV DC
4 10 mV DC
1 DC 0.0mV
250 kS/s
STOPPED


16-Mar-00
16:06:05
CHANGE PARAM
1 20 ms 10.0mV
2 20 ms 10.0mV
3 20 ms 10.0mV
4 20 ms 10.0mV
On line
1 2 3 4 5
Category
All
Cyclic
Dual
Horizontal
Misc
DELETE ALL PARAMETERS
measure
period
phase
pkpk
pks
points
of
1 2 3 4
A B C D
53 sweeps: average low high sigma
pkpk(1) 3.2mV 3.1 3.7 0.2
pkpk(2) 3.0mV 2.5 3.1 0.2
pkpk(3) 3.0mV 2.8 3.4 0.2
pkpk(4) 3.1mV 2.8 3.4 0.2
20 ms
1 10 mV DC
2 10 mV DC
3 10 mV DC
4 10 mV DC
PeaK to PeaK
difFerence between maximum and minimum data values
250 kS/s
STOPPED



- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.
- Record the four **high pkpk** parameter values in Table 4, and compare the test results to the limits in the test record.
- Repeat the test for Time base : **1 msec/div.**
- Record the measurements (high pkpk of 1,2,3,4) in Table 4, and compare the results to the limits in the test record.

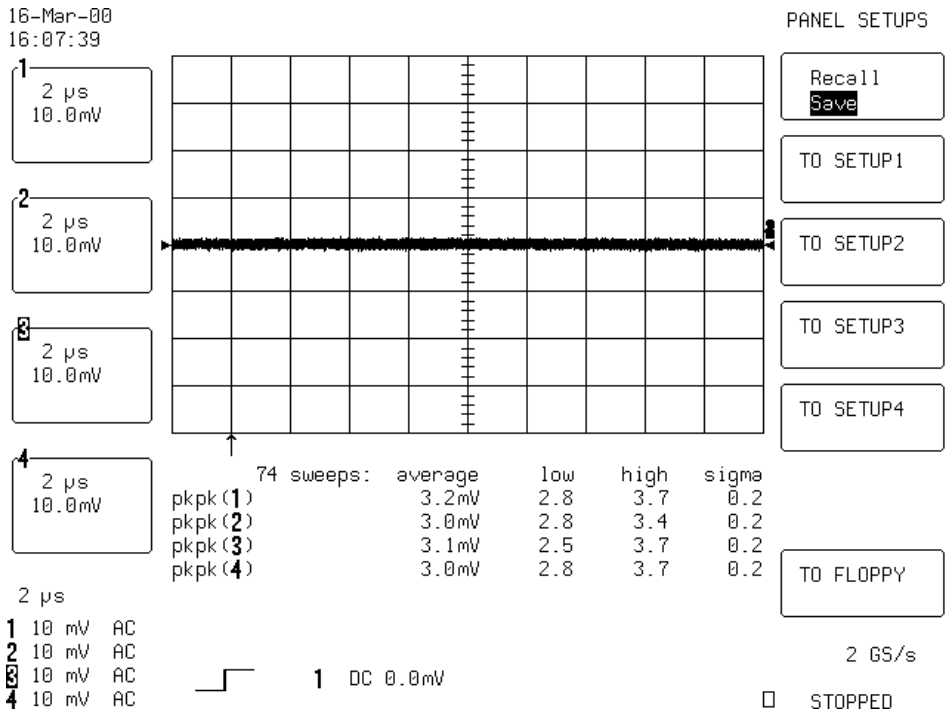
b. AC 1MΩ

- Recall **LC564D019.PNL** or configure the DSO as shown in 5.6.1.a, and for each Channel make the following changes :

  Input Coupling : **AC 1MΩ** on all 4 Channels

  Time base : **2 µsec/div**

- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.
- Record the four **high pkpk** parameter values in Table 4, and compare the test results to the limits in the test record.



c. DC 50Ω

- Recall **LC564D020.PNL** or configure the DSO as shown in 5.6.1.a, and for each Channel make the following changes :

  Input Coupling : **DC 50Ω** on all 4 Channels

  Time base : **2 µsec/div**

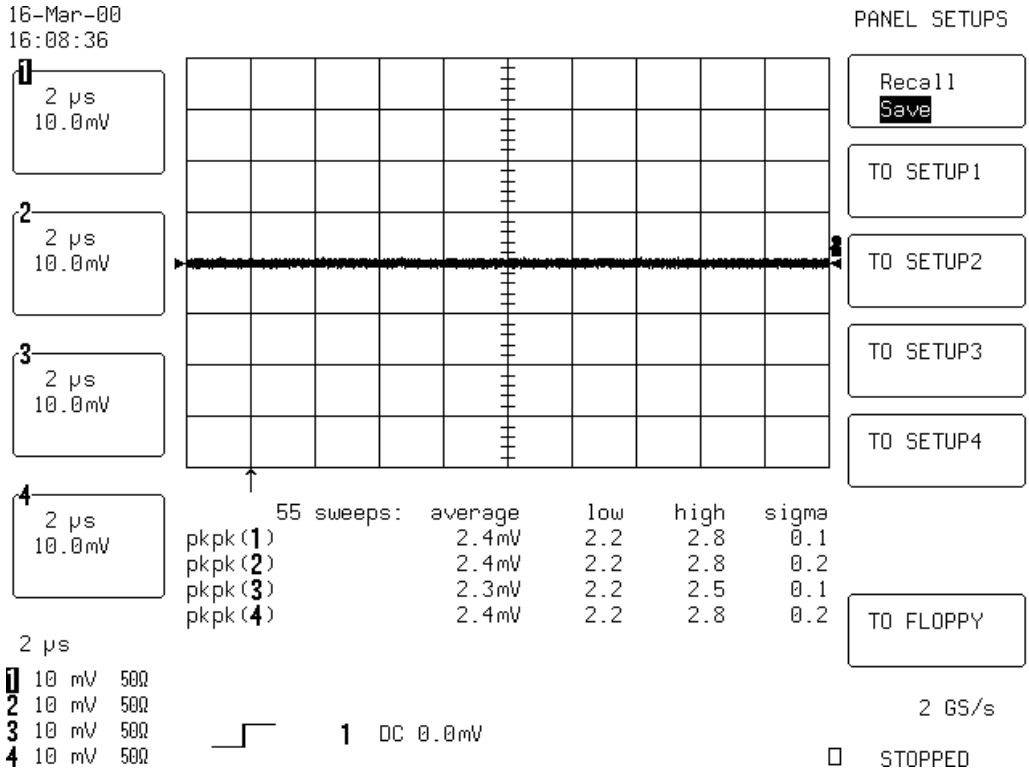
- Press **Clear Sweeps.**

- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.

- Record the four **high pkpk** parameter values in Table 4, and compare the test results to the limits in the test record.

- Repeat the test for Time base: **20 µsec/div.**

- Record the measurements (high pkpk of 1,2,3,4) in Table 4, and compare the results to the limits in the test record.



d. DC 50Ω, 2 Channel Mode

Channel 2 & Channel 3

- Recall **LC564D021.PNL** or configure the DSO as shown in 5.6.1.a**.** and make the following changes :

Input Coupling : **DC 50Ω** on all 4 Channels

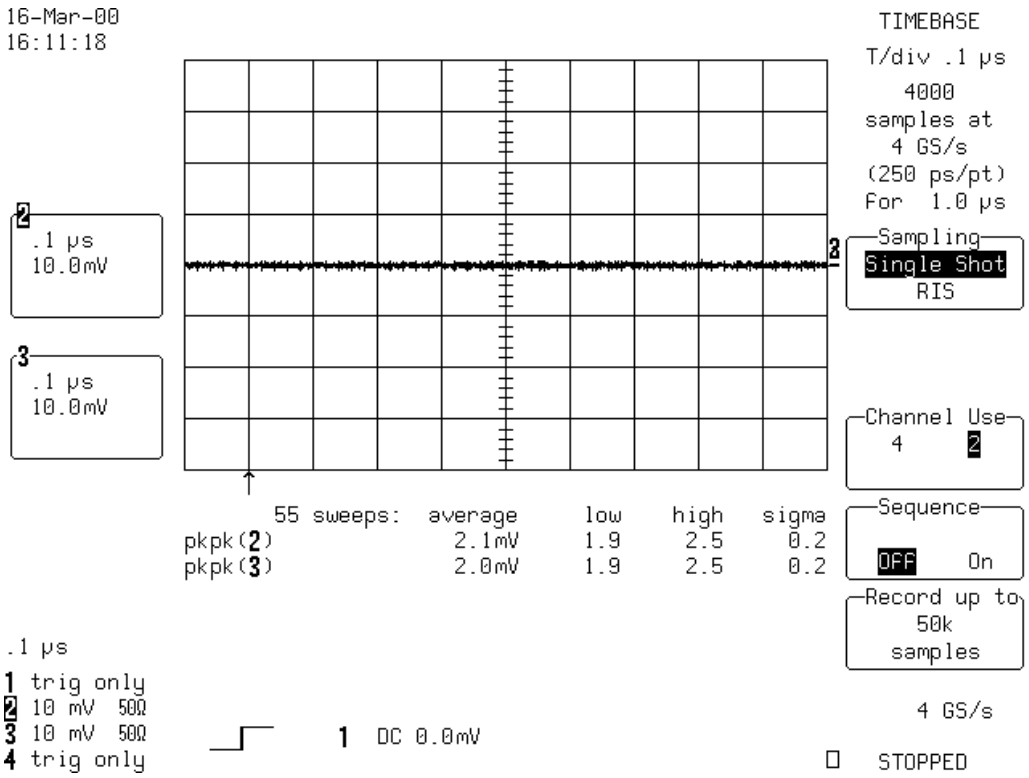
Input gain : **10 mV/div.** on all 4 Channels

Channels Trace ON **Channel 2**, **Channel 3**
Channels Trace OFF **Channel 1**, **Channel 4**
Time base : **1 µsec/div.**

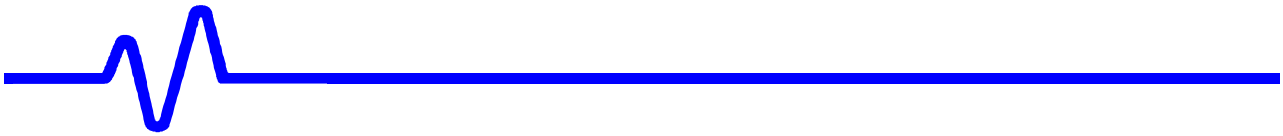
Select Time base Setup

Channel use : **2**

Press : **Cursors/Measure**
Change parameters
On line 1 : **Measure pkpk of Ch2**
On line 2 : **Measure pkpk of Ch3**



- Check that the Sampling rate is **4 GS/s**
- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.
- Record the two **high pkpk of Ch2 & Ch3** in Table 4, and compare the test results to the limits in the test record.



5.6.2 Rms Noise

Specifications

0.9 % of full scale or 0.72 mV at 10 mV/div.

a. DC 1MΩ

Procedure

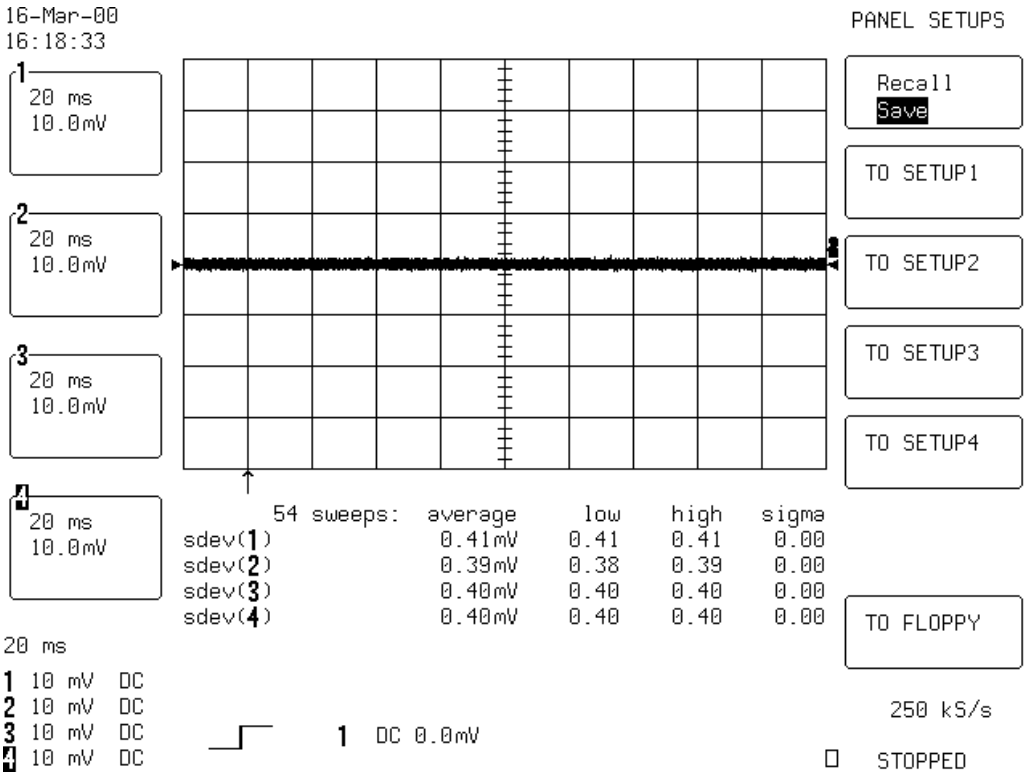
With no signal connected to the inputs

- Recall **LC564D024.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	**10 mV/div.** on all 4 Channels
Input Offset	:	**0mv** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**1**
Coupling 1	:	**DC**
Trigger Mode	:	**Auto**
Time base	:	**20 msec/div.**
Channel use	:	**4**
Record up to	:	**50 k Samples**
Press	:	**Cursors/Measure**
Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**On**

Change parameters

Category	:	**All**
On line 1	:	**Measure sdev of Ch1**
On line 2	:	**Measure sdev of Ch2**
On line 3	:	**Measure sdev of Ch3**
On line 4	:	**Measure sdev of Ch4**
On line 5	:	**no parameter selected for line 5**



- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.
- Record the four **high sdev** parameter values in Table 5, and compare the test results to the limits in the test record.
- Repeat the test for Time base : **1 msec/div.**
- Record the measurements (high sdev of 1,2,3,4) in Table 5, and compare the results to the limits in the test record.

b. AC 1MΩ

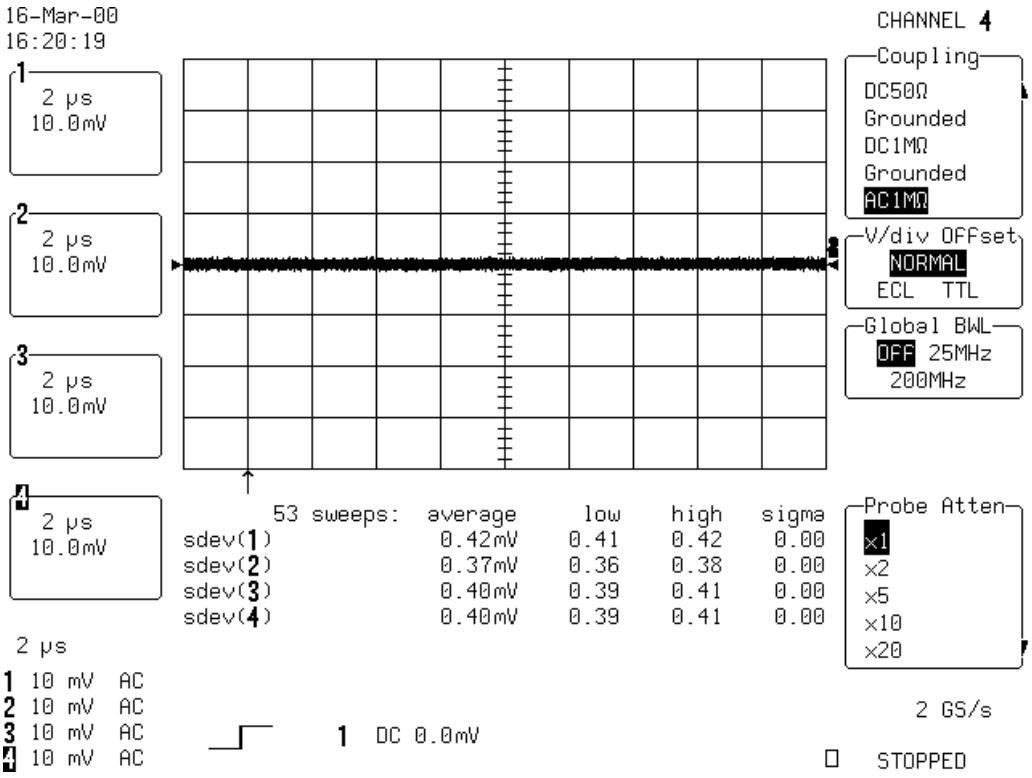
- Recall **LC564D025.PNL** or configure the DSO as shown in 5.6.2.a. and for each Channel make the following change :

  Input Coupling : **AC 1MΩ** on all 4 Channels

  Time base : **2 µsec/div.**

- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.

- Record the four **high sdev** parameter values in Table 5, and compare the test results to the limits in the test record.



c. DC 50Ω

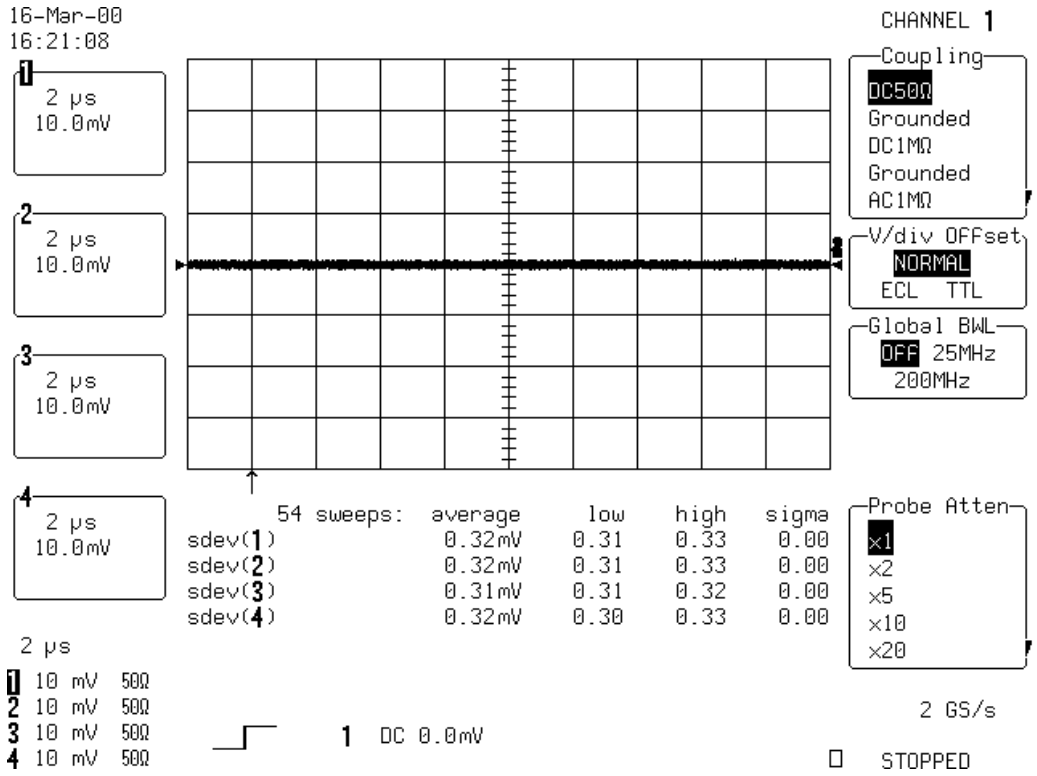
- Recall **LC564D026.PNL** or configure the DSO as shown in 5.6.2.a and make the following changes :

  Input Coupling : **DC 50Ω** on all 4 Channels

  Time base : **2 µsec/div.**

- Press **Clear Sweeps.**

- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.



- Record the four **high sdev** parameter values in Table 5, and compare the test results to the limits in the test record.

- Repeat the test for Time base : **20 µsec/div.**

- Record the measurements (high sdev of 1,2,3,4) in Table 5, and compare the results to the limits in the test record.

d. DC 50Ω, 2 Channel Mode

Channel 2 & Channel 3

- Recall **LC564D027.PNL** or configure the DSO as shown in 5.6.2.a**.** and make the following changes :

  Input Coupling : **DC 50Ω** on all 4 Channels

  Input gain : **10 mV/div.** on all 4 Channels

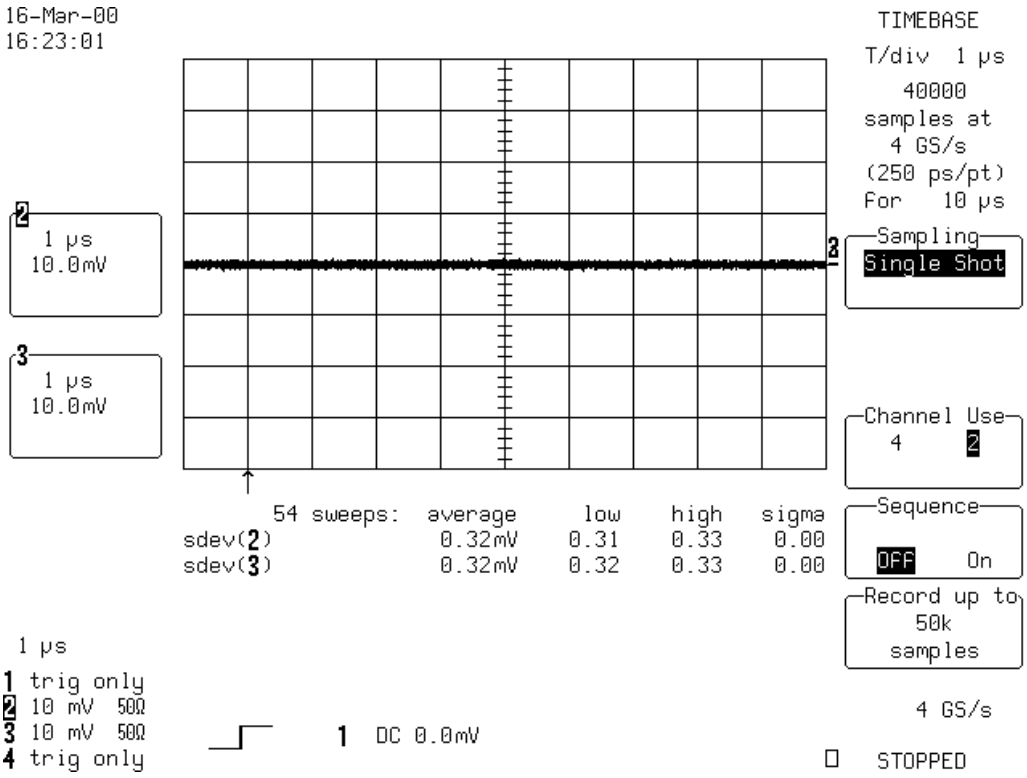
  Channels Trace ON **Channel 2**, **Channel 3**
  Channels Trace OFF **Channel 1**, **Channel 4**

  Time base : **1 µsec/div.**

Select Time base Setup
Channel use : **2**

Press : **Cursors/Measure**
Change parameters
On line 1 : **Measure sdev of Ch2**

On line 2 : **Measure sdev of Ch3**



- Check that the Sampling rate is **4 GS/s**
- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.
- Record the two **high sdev of Ch2 & Ch3** in Table 5, and compare the test results to the limits in the test record.

5.6.3 Ground Line Test

Specifications

±5 % of full scale at 2 mV/div.
±3 % of full scale at 5 mV/div.
±2 % of full scale at 10 mV/div. and above.

Procedure

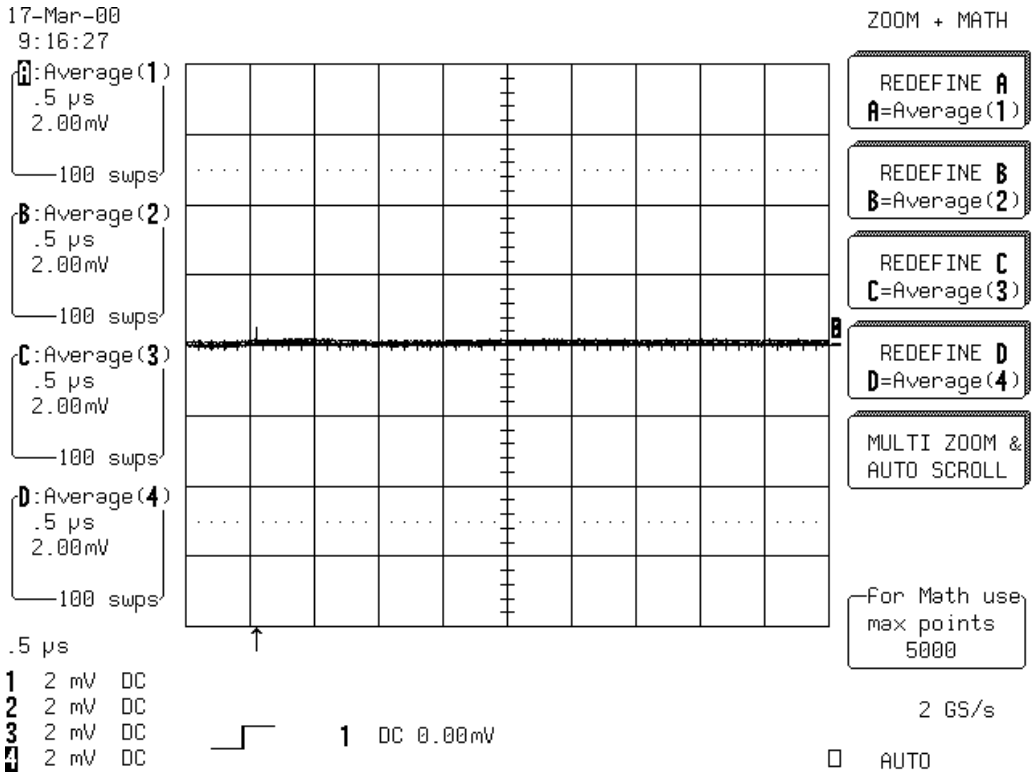
The stability of the ground line is verified for each channel at each fixed gain. The measured average values are checked against the desired limits.

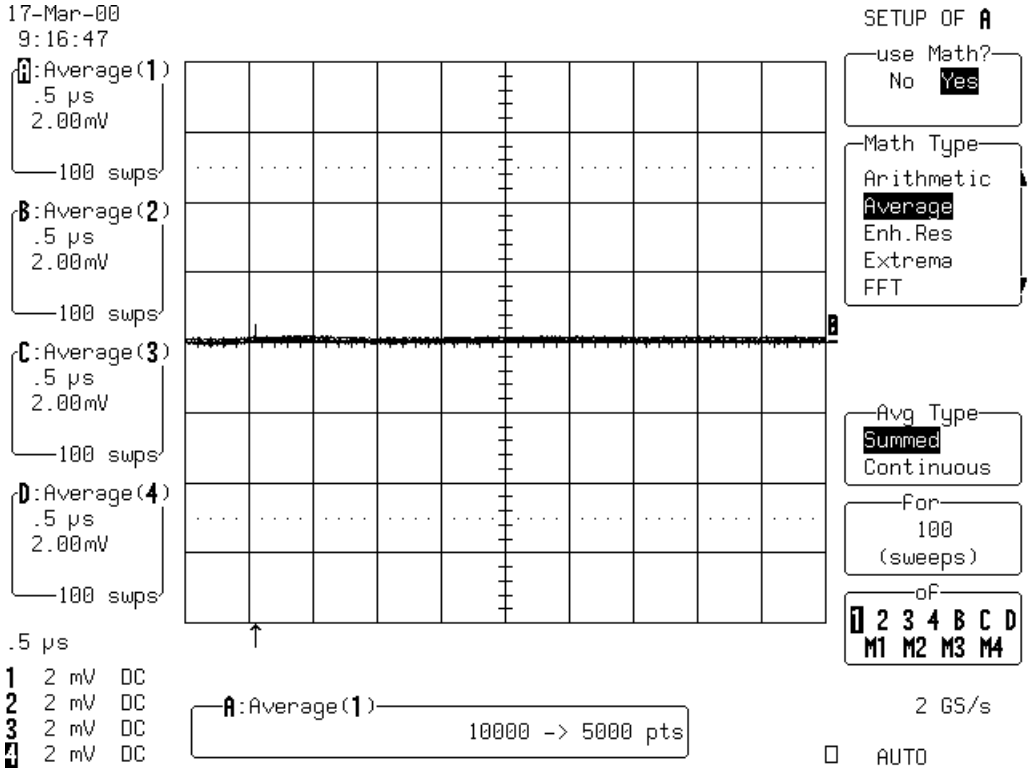
a. DC 1MΩ

With no signal connected to the inputs

- Recall **LC564D029.PNL** or configure the DSO :

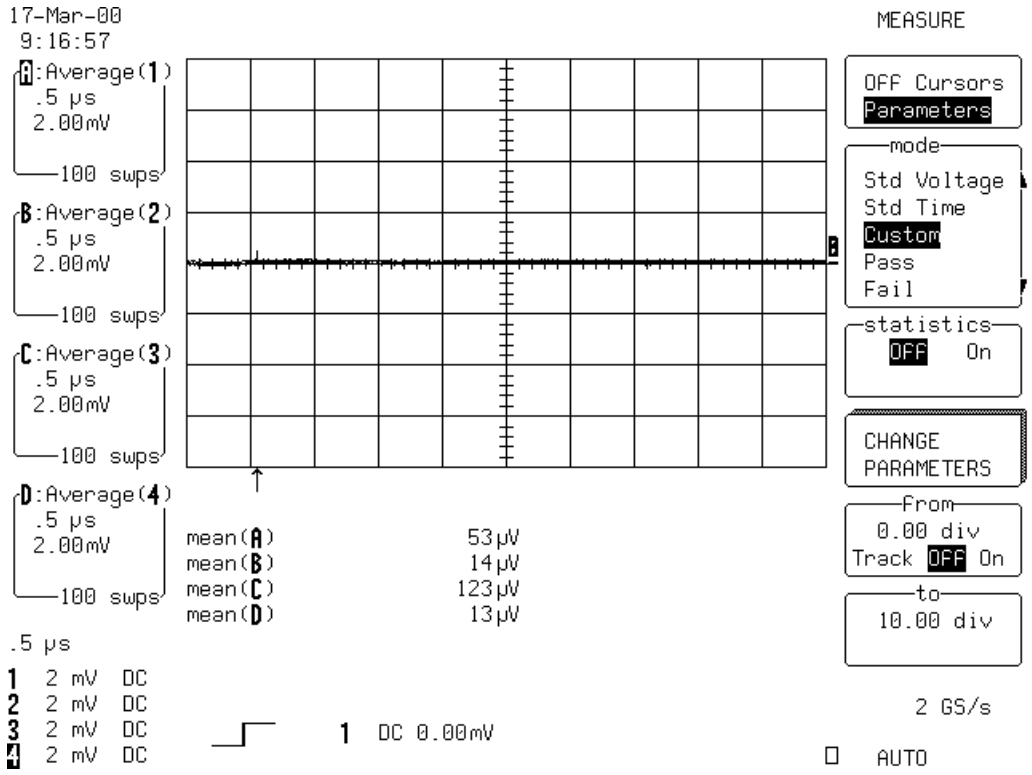
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	from **2mV/div** to **1 V/div. (see Table 6)** on all 4 Ch
Offset	:	**Zero** on all 4 Channels
Trigger on	:	**Channel 1, DC**
Trigger mode	:	**Auto**
Time base	:	**0.5 µsec/div.**
Channel use	:	**4**
Record up to	:	**50 k**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
Zoom+Math Trace ON		**A, B, C & D**
Select Math Setup		
For Math	:	**Use at most 5000 points**
Redefine A, B, C, D		**Channel 1, Channel 2, Channel 3 & Channel 4**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**100 sweeps**
Press	:	**Cursors/Measure**
Select	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**off**


17-Mar-00
9:16:27
A:Average(1)
.5 µs
2.00mV
100 swps
B:Average(2)
.5 µs
2.00mV
100 swps
C:Average(3)
.5 µs
2.00mV
100 swps
D:Average(4)
.5 µs
2.00mV
100 swps
.5 µs
1 2 mV DC
2 2 mV DC
3 2 mV DC
4 2 mV DC
1 DC 0.00mV
ZOOM + MATH
REDEFINE A
A=Average(1)
REDEFINE B
B=Average(2)
REDEFINE C
C=Average(3)
REDEFINE D
D=Average(4)
MULTI ZOOM &
AUTO SCROLL
For Math use
max points
5000
2 GS/s
AUTO


17-Mar-00
9:16:47
A:Average(1)
.5 µs
2.00mV
100 swps
B:Average(2)
.5 µs
2.00mV
100 swps
C:Average(3)
.5 µs
2.00mV
100 swps
D:Average(4)
.5 µs
2.00mV
100 swps
.5 µs
1 2 mV DC
2 2 mV DC
3 2 mV DC
4 2 mV DC
A:Average(1)
10000 -> 5000 pts
SETUP OF A
use Math?
No Yes
Math Type
Arithmetic
Average
Enh.Res
Extrema
FFT
Avg Type
Summed
Continuous
For
100
(sweeps)
of
1 2 3 4 B C D
M1 M2 M3 M4
2 GS/s
AUTO

Change parameters

On line 1	:	**Measure mean of A**
On line 2	:	**Measure mean of B**
On line 3	:	**Measure mean of C**
On line 4	:	**Measure mean of D**

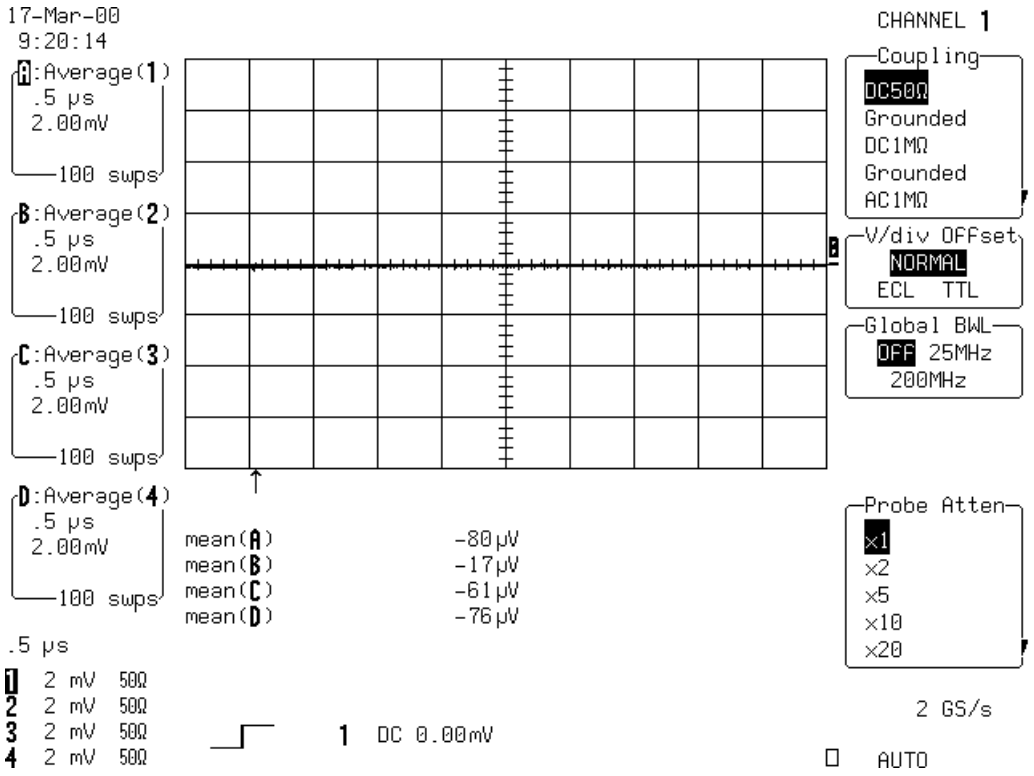


- Press **Clear Sweeps.**
- After **100 sweeps** record the **mean** value of **A, B, C & D** in Table 6, and compare the test results to the limits in the test record.
- Repeat step 5.6.3.a. for all vertical scale settings listed in Table 6, and check that the test results (mean value of A, B, C, D) are within the limits specified.
- Record the measurements in Table 6.

b. DC 50Ω

- Recall **LC564D030.PNL** or configure the DSO as shown in 5.6.3.a. and for each Channel make the following change:

  Input Coupling : **DC 50Ω** on all 4 Channels
  Input gain : from **2mV/div** to **.2 V/div. (see Table 7)** on all 4 Ch



- Press **Clear Sweeps.**

- After **100 sweeps** record the **mean** value of **A, B, C & D** in Table 7, and compare the test results to the limits in the test record.

- Repeat step 5.6.3.b. for all vertical scale settings listed in Table 7, and check that the test results (mean value of A, B, C, D) are within the limits specified.

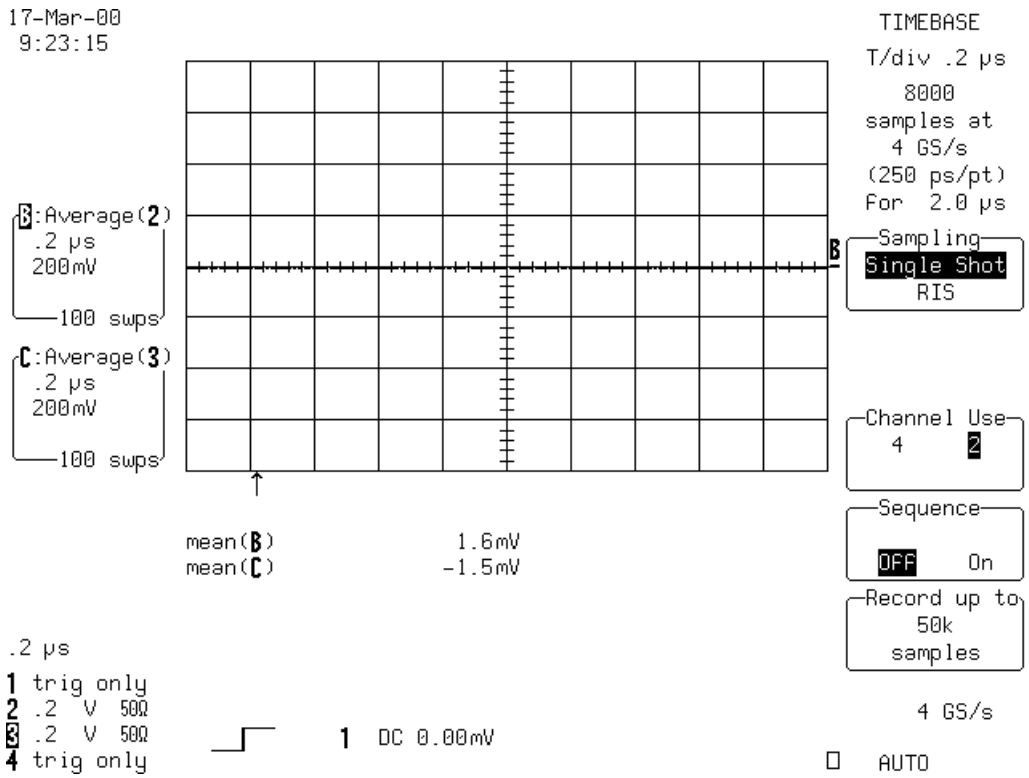
- Record the measurements in Table 7.

c. DC 50Ω, 2 Channel Mode

Channel 2 & Channel 3

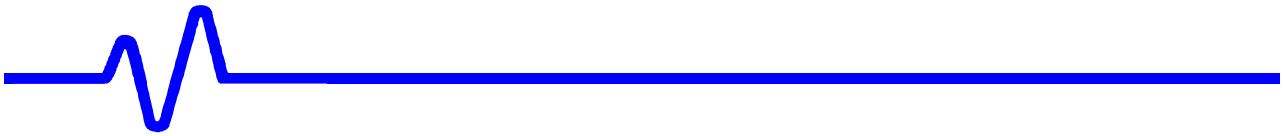
- Recall **LC564D031.PNL** or configure the DSO as shown in 5.6.3.a. and make the following change :

Input Coupling	:	**DC 50Ω** on all 4 Channels
Input gain	:	**0.2 V/div.** on all 4 Channels
Trace ON	:	**A:Average of (2), C:Average of (3)**
Trace OFF	:	**B:Average of (1), D:Average of (4)**
Time base	:	**0.2 µsec/div.**
Select Time base Setup		
Channel use	:	**2**
Press	:	**Cursors/Measure**
Change parameters		
On line 1	:	**Mean of B**
On line 2	:	**Mean of C**
On line 3, 4, 5	**:**	**No parameter selected**



- Check that the Sampling rate is **4 GS/s**
- Press **Clear Sweeps.**

- After **100 sweeps** record the **mean** value of **B & C** in Table 7, and compare the test results to the limits in the test record.



5.7 DC Accuracy

Specification

≤ ±5 % of full scale at 2mV/div, with 0 mV offset.
≤ ±3 % of full scale at 5mV/div, with 0 mV offset.
≤ ±2 % of full scale at 10mV/div and above, with 0 mV offset.

Description

This test measures the DC Accuracy within the gain range specified.
It requires a DC source with a voltage range of 0 V to 20 V adjustable in steps of no more than 15 mV, and a calibrated DMM that can measure voltage to 0.1 %.
Measurements are made using voltage values applied by the external voltage reference source, measured by the DMM, and in the oscilloscope using the parameters Std voltage.
For each known input voltage, the deviation is checked against the tolerance.

5.7.1 Positive DC Accuracy

a. DC 50Ω

Procedure

- Recall **LC564D045.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 50Ω** on all 4 Channels
Input offset	:	**0.0 mV** on all 4 Channels
Input gain	:	from **2mV/div to 1 V/div.** (see Table 9) on all 4 Ch
Trigger setup	:	**Edge**
Trigger on	:	**Line**
Slope line	:	**Positive**
Mode	:	**Auto**
Time base	:	**2 msec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
Zoom+Math Trace ON		**A, B, C & D**
Select Math Setup		
For Math	:	**Use at most 5000 points**
Redefine A, B, C, D		**Channel 1, Channel 2, Channel 3 & Channel 4**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**

For	:	**100 sweeps**
Cursors/Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**off**

Change parameters

On line 1	:	**Measure mean of A**
On line 2	:	**Measure mean of B**
On line 3	:	**Measure mean of C**
On line 4	:	**Measure mean of D**

- For the low sensitivities: **2 mV, 5 mV, 10 mV and 20 mV/div**., connect the test equipment as shown in Figure 5-1.

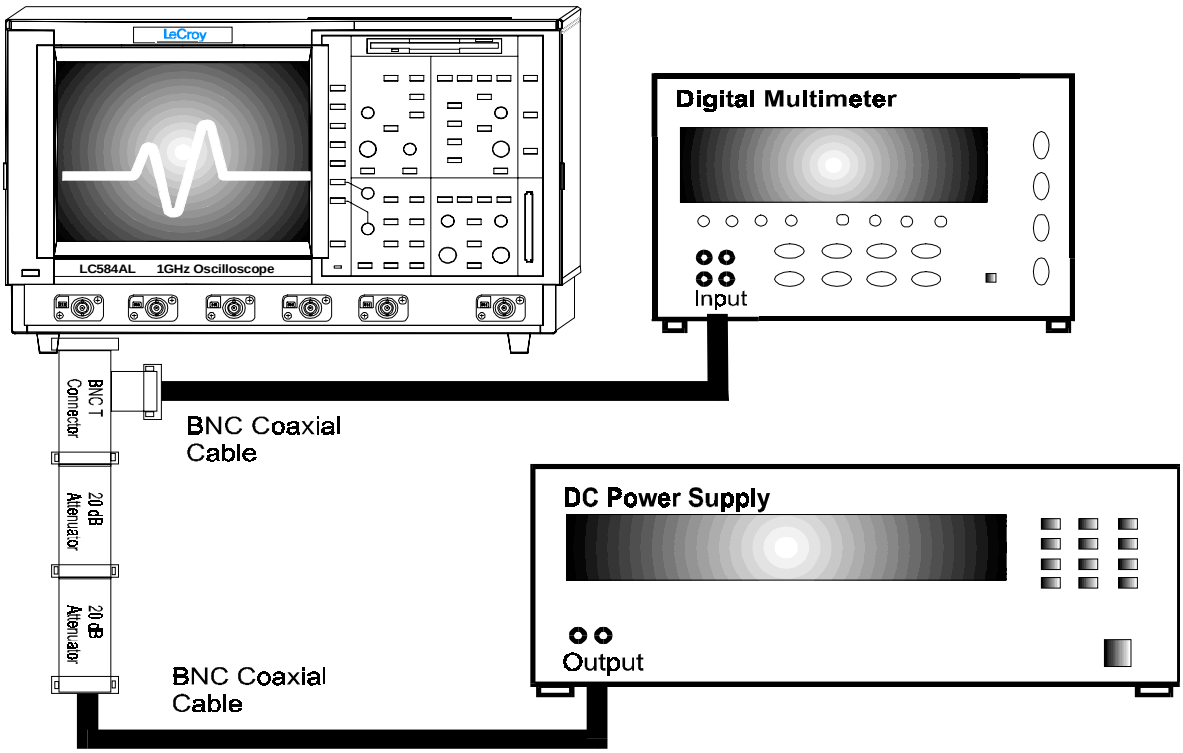


Figure 5-1 : DC 50Ω Accuracy Equipment Setup for 2, 5, 10 and 20 mV/div

- For the sensitivities : **50 mV** and **100 mV/div**, connect the test equipment as shown in Figure 5-2.

- For the range **1 V/div** no attenuator is required, connect the test equipment as shown in Figure 5-3.

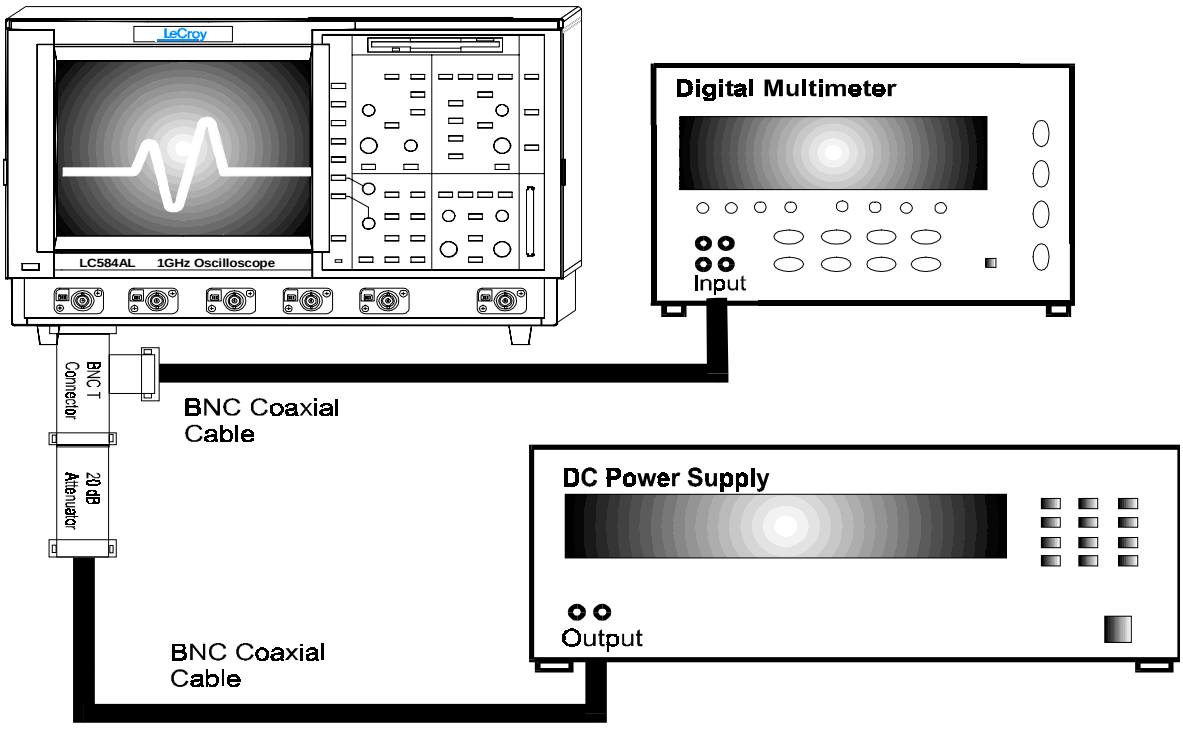


Figure 5-2 : DC 50Ω Accuracy Equipment Setup for 50 and 100 mV/div

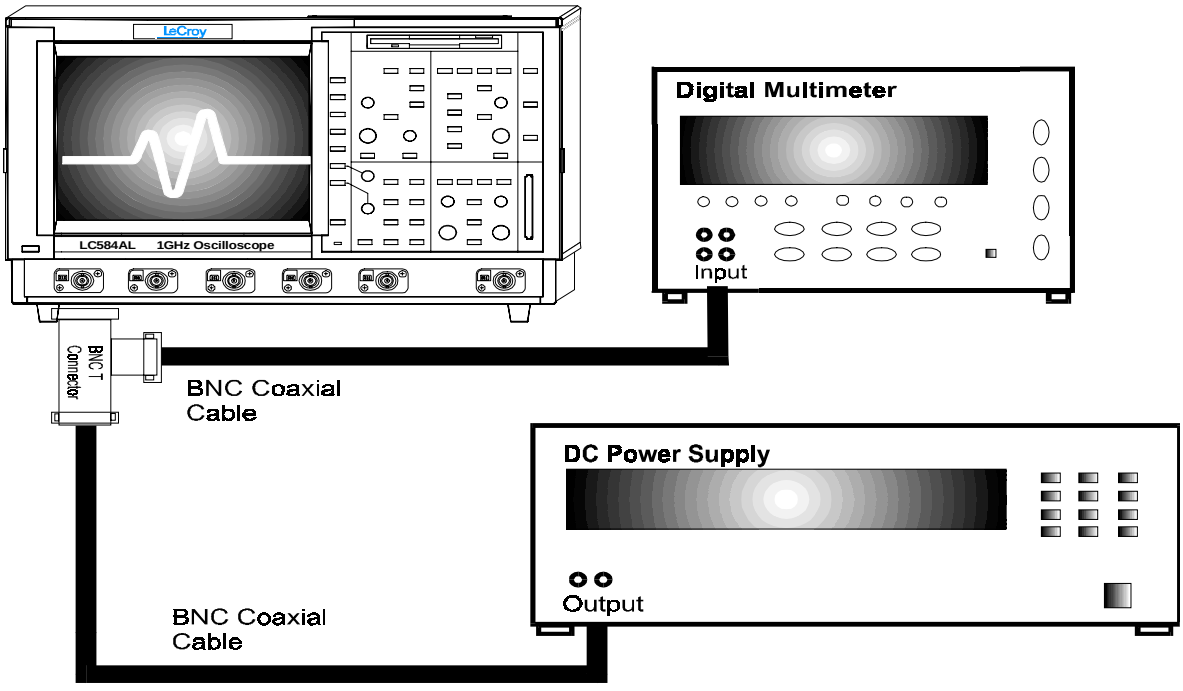


Figure 5-3 : DC 50Ω Accuracy Equipment Setup for 1 V/div.

- For each **DSO Volts/div**, set the output of the external **DC voltage reference source** as shown in Table 8, column PS output.

  1) Connect the DMM and record the **voltage reading** in Table 8, column **DMM.**

  2) Disconnect the DMM from the BNC T connector.

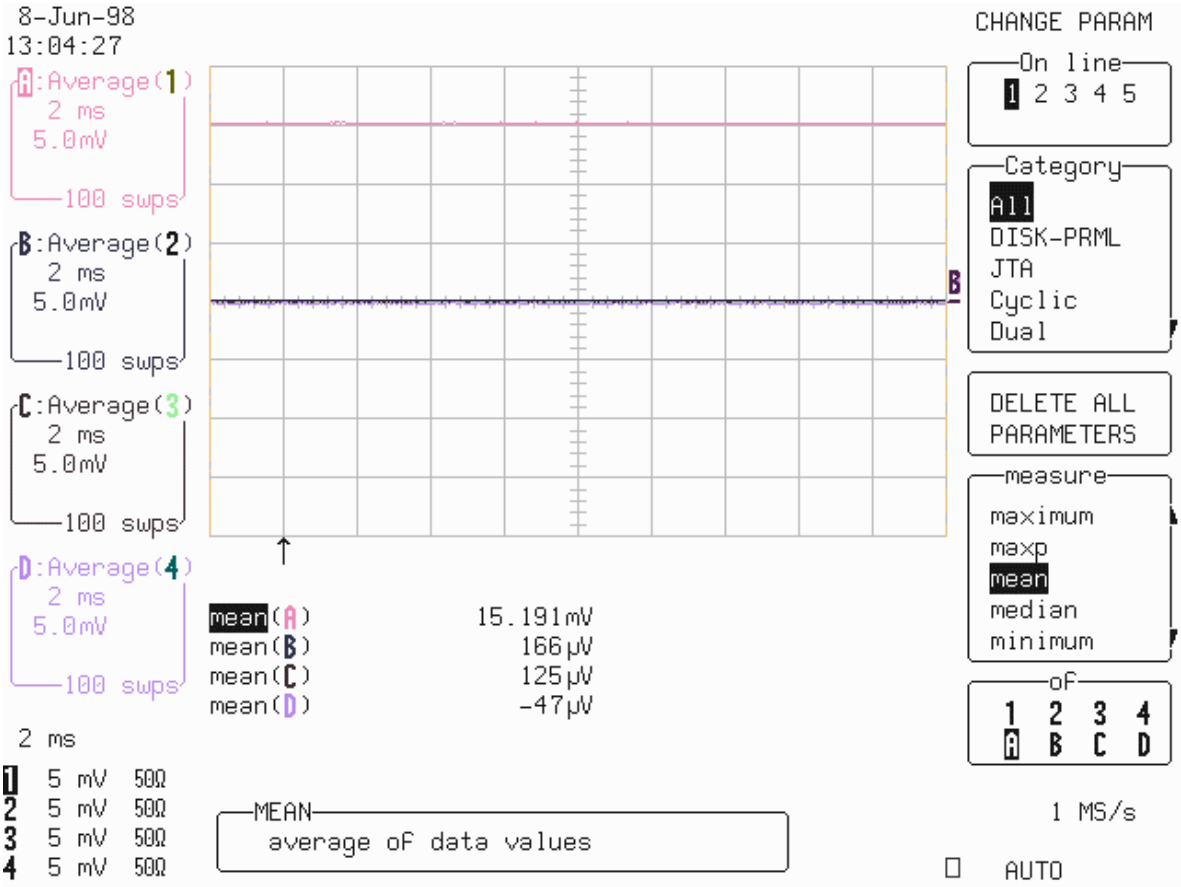
  3) Press **Clear Sweeps**

  4) After 100 sweeps, read off the **DSO mean parameter**, and record the measurement in Table 8, column **Mean**.

- For each DC voltage applied to the DSO input, repeat parts 1), 2), 3) and 4).

- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading. Record the test result in Table 8, and compare the **Difference (Δ)** to the corresponding limit in the test record.

- Repeat step 5.7.1.a. for the other channels, substituting channel controls and input connector.



b. DC 1MΩ

Procedure

- Recall **LC564D046.PNL** or configure the DSO as shown in 5.7.1.a. and make the following change :

  Input gain : **5mV/div, 0.1 V/div, and 2V/dv** (see Table 10) on all 4 Ch
  Input Coupling : **DC 1MΩ** on all 4 Channels

- For 5 mV/div., connect the test equipment as shown in Figure 5-4.

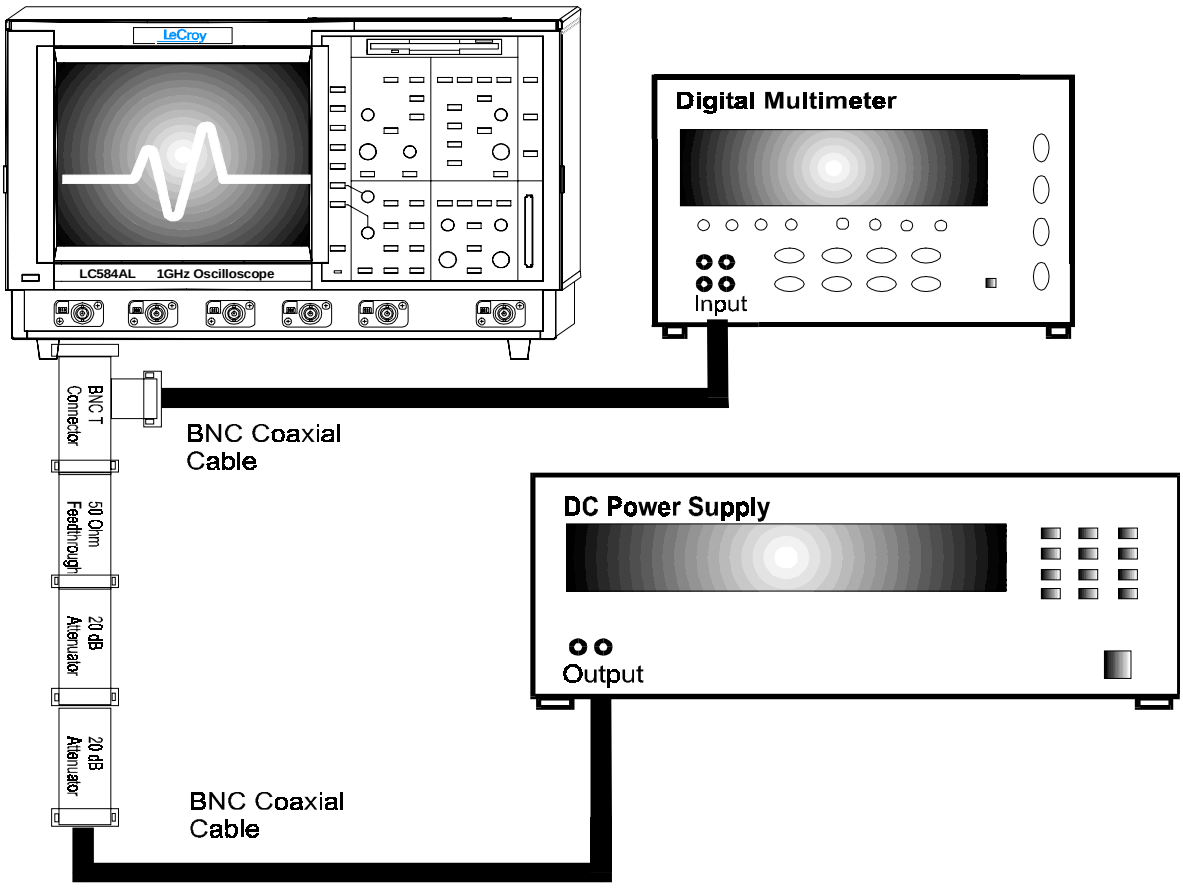


Figure 5-4: DC 1MΩ Accuracy Equipment Setup for 5 mV/div.

- For 100 mV/div, connect the test equipment as shown in Figure 5-5.

- For 2V/div no attenuator is required, connect the test equipment as shown in Figure 5-6.

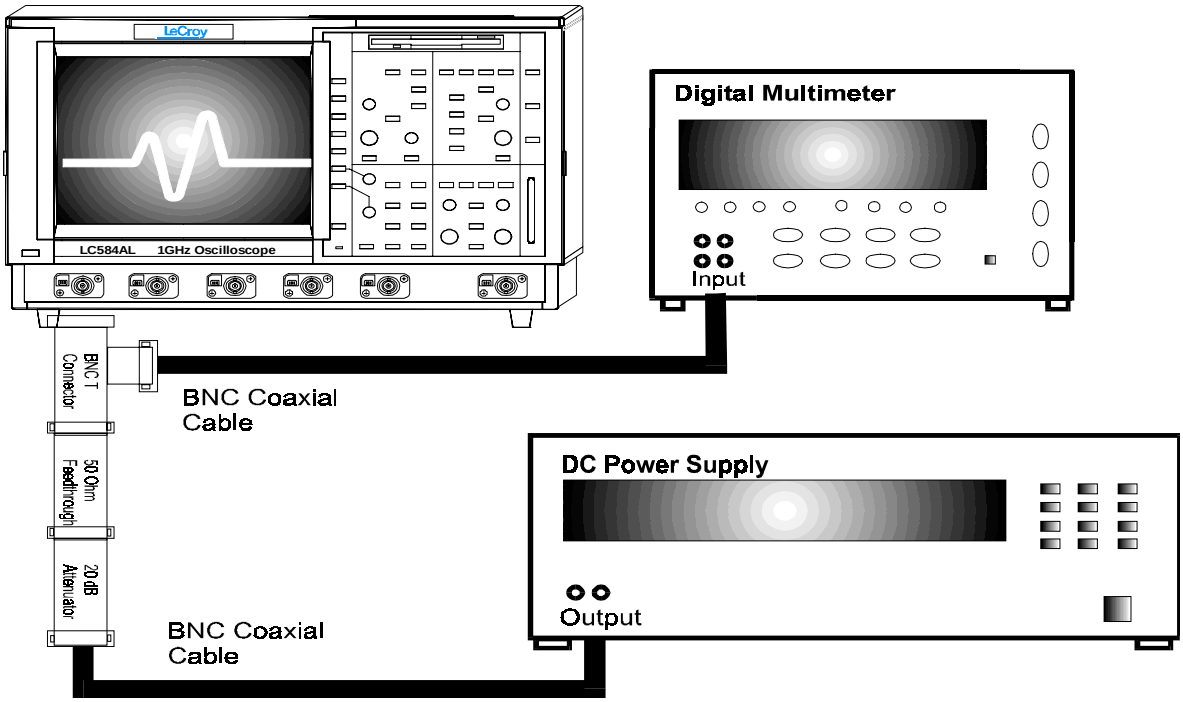


Figure 5-5 : DC 1MΩ Accuracy Equipment Setup for 100 mV/div

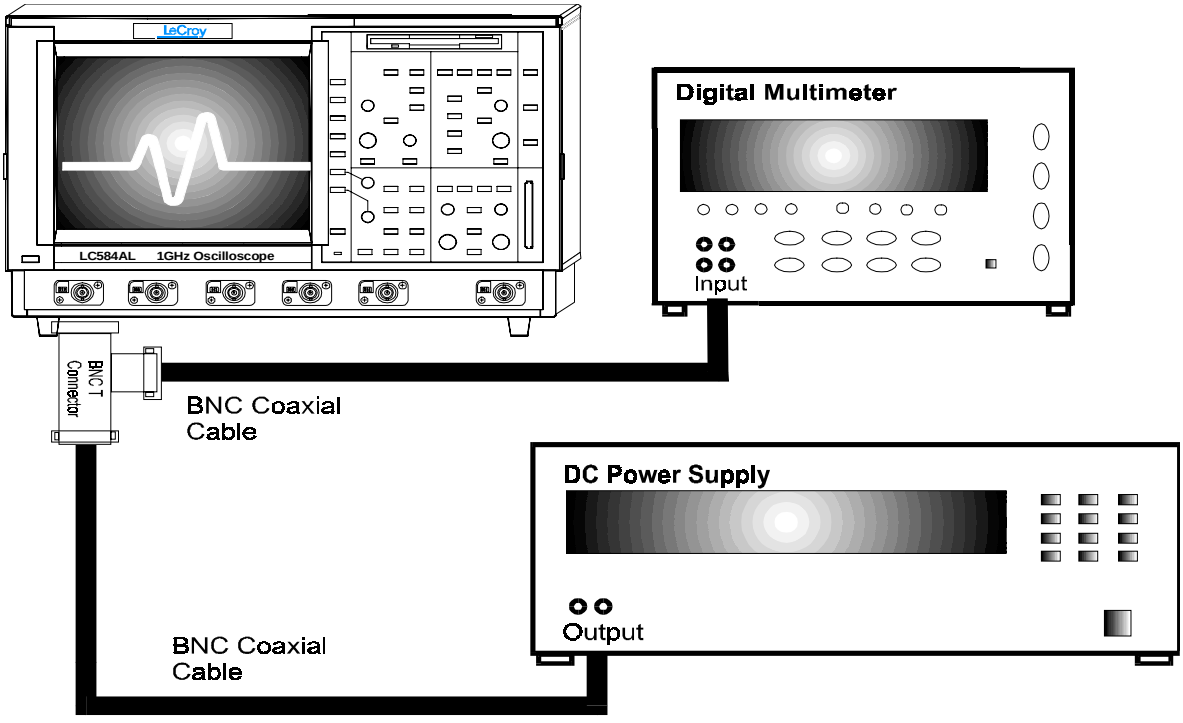


Figure 5-6 : DC 1MΩ Accuracy Equipment Setup for 2V/div.

- For each **DSO Volts/div**, set the output of the external **DC voltage reference source** as shown in Table 9, column PS output.

  1) Connect the DMM and record the **voltage reading** in Table 9, column **DMM.**

  2) Disconnect the DMM from the BNC T connector.

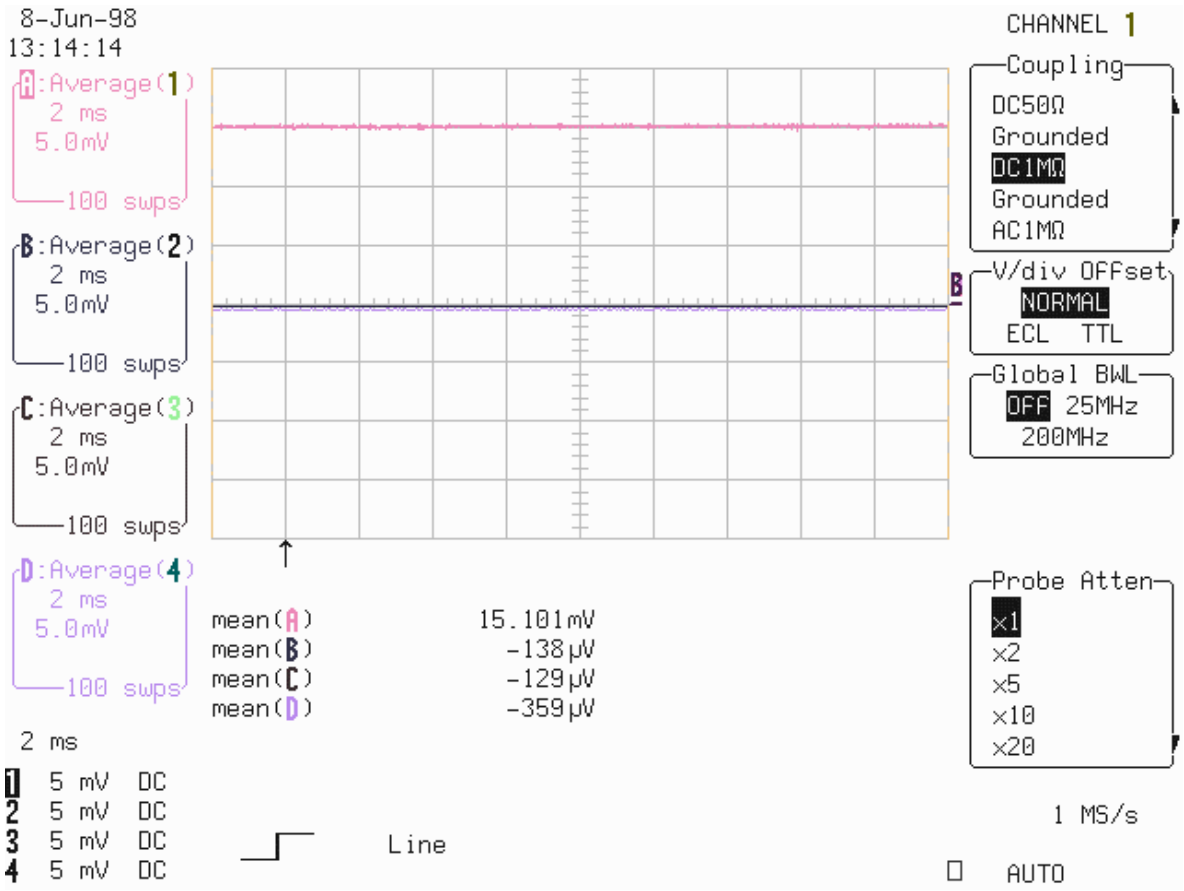
  3) Press **Clear Sweeps**

  4) After 100 sweeps, read off the **DSO mean parameter**, and record the measurement in Table 9, column **Mean**.

- For each DC voltage applied to the DSO input, repeat parts 1), 2), 3) and 4).

- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading. Record the test result in Table 9, and compare the **Difference (Δ)** to the corresponding limit in the test record.

- Repeat step 5.7.1.b. for the other channels, substituting channel controls and input connector.



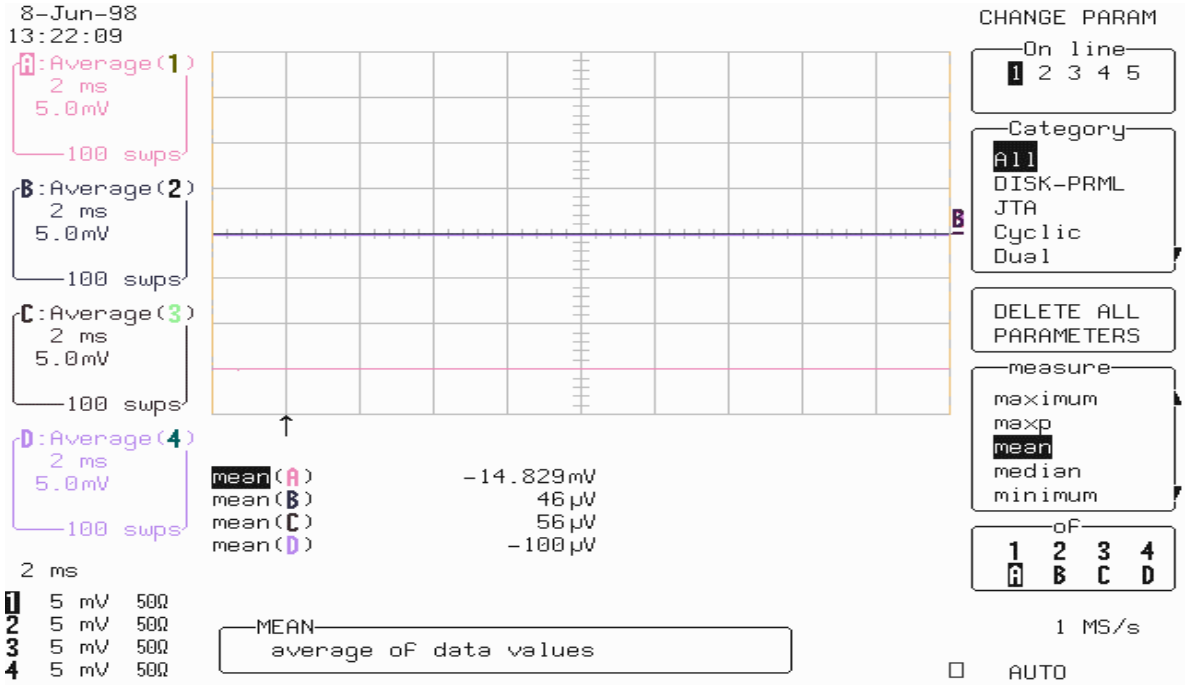
5.7.2 Negative DC Accuracy

a. DC 50Ω

- Recall **LC564D045.PNL** or configure the DSO as shown in 5.7.1.a.
- Connect the test equipment as shown in either Figure 5-1 or 5-2 or 5-3.
- For each **DSO Volts/div**, set the output of the external **DC voltage reference source** as shown in Table 10, column PS output. (if a banana-BNC adapter is being used it can simply be turned to get the opposite polarity)

  1) Connect the DMM and record the **voltage reading** in Table 10, column **DMM.**
  2) Disconnect the DMM from the BNC T connector.
  3) Press **Clear Sweeps**
  4) After 100 sweeps, read off the **DSO mean parameter**, and record the measurement in Table 11, column **Mean**.

- For each DC voltage applied to the DSO input, repeat parts 1), 2), 3) and 4).
- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading. Record the test result in Table 10, and compare the **Difference (Δ)** to the corresponding limit in the test record.
- Repeat step 5.7.2.a. for the other channels, substituting channel controls and input connector.



b. DC 1 MΩ

- Recall **LC564D046.PNL** or configure the DSO as shown in 5.7.1.a. and make the following change :

  Input gain : **5mV/div, 0.1 V/div, and 2V/dv** (see Table 11) on all 4 Ch
  Input Coupling : **DC 1 MΩ** on all 4 Channels

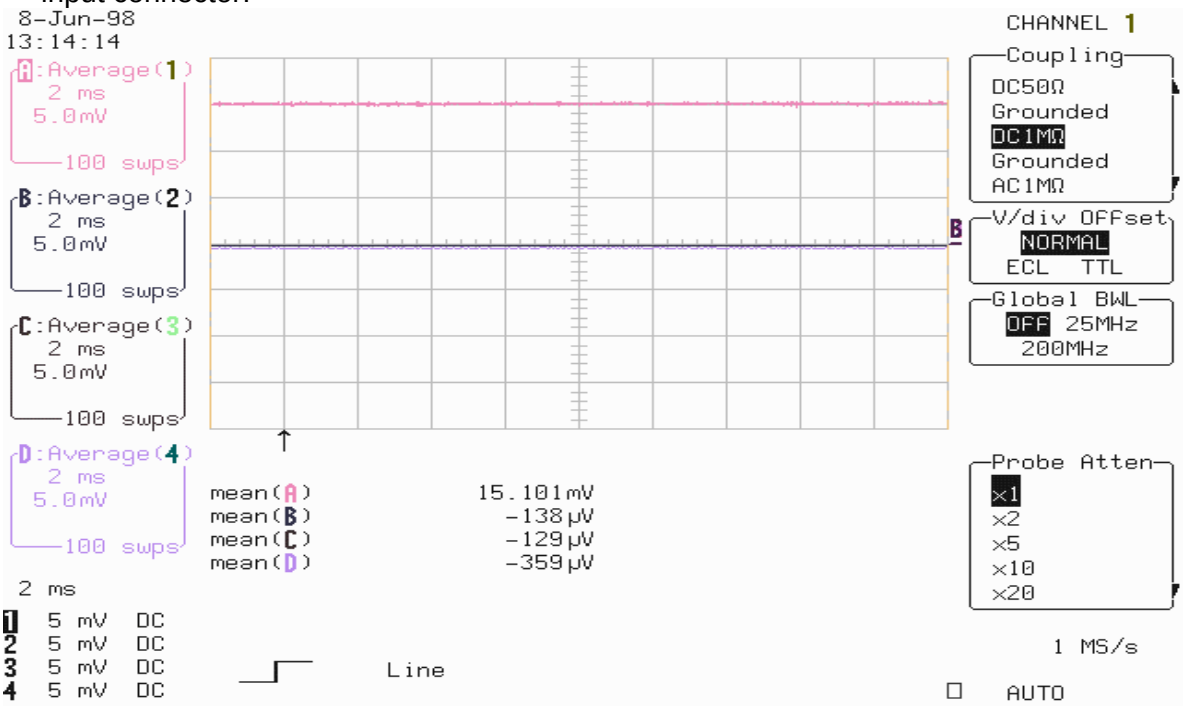
- Connect the test equipment as shown in either Figure 5-4 or 5-5 or 5-6.

- For each **DSO Volts/div**, set the output of the external **DC voltage reference source** as shown in Table 11, column PS output.
  1) Connect the DMM and record the **voltage reading** in Table 11, column **DMM.**
  2) Disconnect the DMM from the BNC T connector.
  3) Press **Clear Sweeps**
  4) After 100 sweeps, read off the **DSO mean parameter**, and record the measurement in Table 11, column **Mean**.

- For each DC voltage applied to the DSO input, repeat parts 1), 2), 3) and 4).

- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading. Record the test result in Table 11, and compare the **Difference (Δ)** to the corresponding limit in the test record.

- Repeat step 5.7.2.b. for the other channels, substituting channel controls and input connector.



5.8 Offset Accuracy

Specifications

Offset range at 2 mV/div: ±0.4Volt, Accuracy ≤ ±4.8 mV (5% of FS + 1% of offset).
Offset range at 5 mV/div: ±1Volt, Accuracy ≤ ±11.2 mV (3% of FS +1% of offset).

Description

The offset test is done at 2 mV/div and 5 mV/div for 50Ω and at 5 mV/div for 1MΩ coupling, with a signal of ±0.4 Volt or ±1 Volt cancelled by an offset of the opposite polarity.

5.8.1 Positive Offset Accuracy

a. DC 50Ω

Procedure

- Recall **LC564D047.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 50Ω** on all 4 Channels
Input gain	:	**2mV/div** on all 4 Channels
Input offset	:	**+0.4 Volt** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**Line**
Coupling 1	:	**DC**
Mode	:	**Auto**
Time base	:	**2 msec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
Zoom+Math Trace ON		**A, B, C & D**
Select Math Setup		
For Math	:	**Use at most 5000 points**
Redefine A, B, C, D		**Channel 1, Channel 2, Channel 3 & Channel 4**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**100 sweeps**
Cursors/Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**off**
Change parameters		

On line 1	:	**Measure mean of A**
On line 2	:	**Measure mean of B**
On line 3	:	**Measure mean of C**
On line 4	:	**Measure mean of D**

- Connect the test equipment as shown in Figure 5-7.

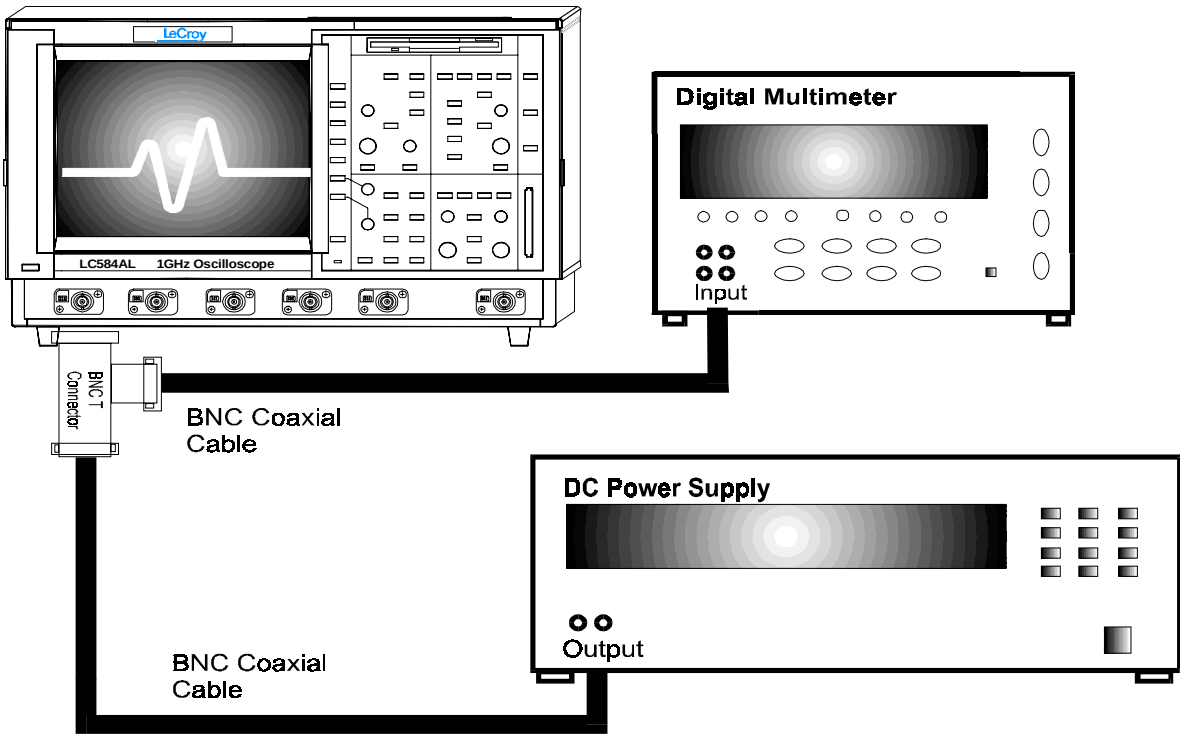


Figure 5-7 : Offset Accuracy Equipment Setup

- Set the output of the external **DC voltage reference source** to **–0.4 Volt.**

  1) Verify that the displayed trace A : Average (1) is on the screen, near the center horizontal graticule line. If the trace is not visible, modify the **DC voltage reference source output** until the trace is within ± 2 divisions of center.

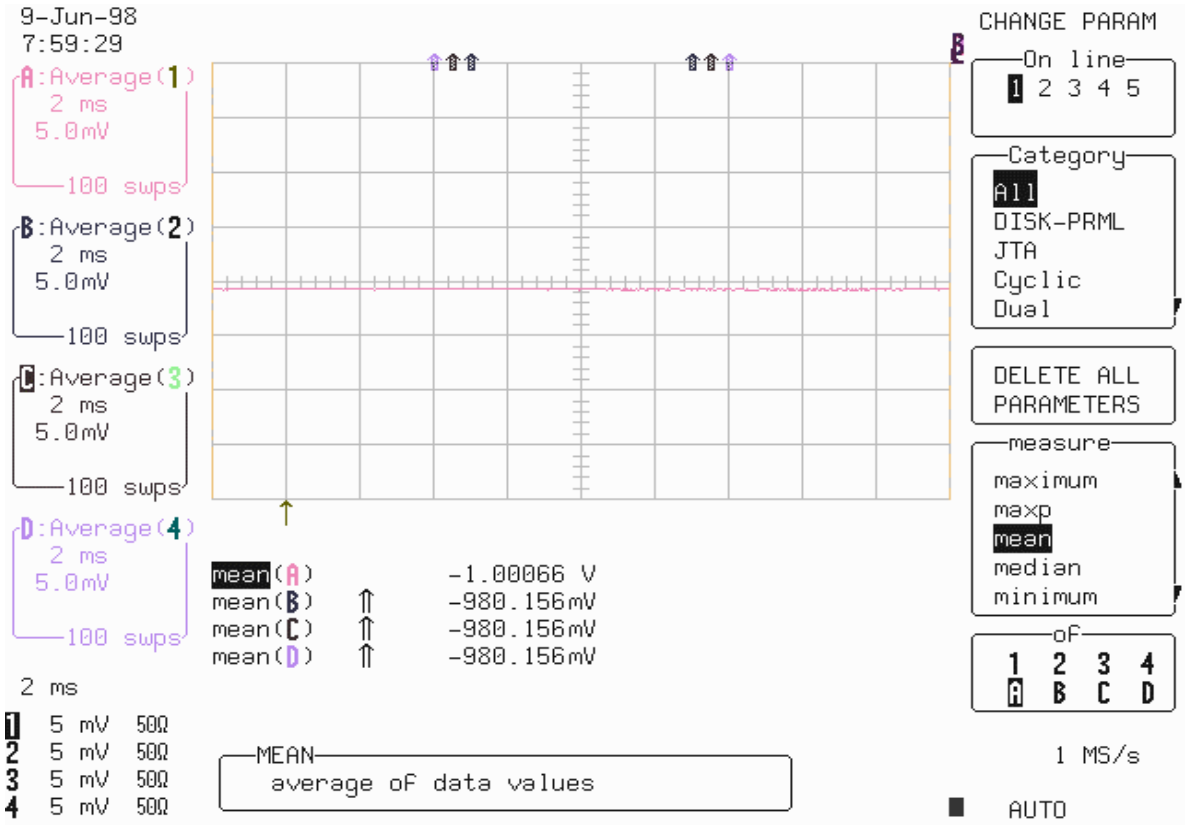
  2) Connect the DMM and record the **voltage reading** in Table 12, column **DMM**.

  3) Disconnect the DMM from the BNC T connector.

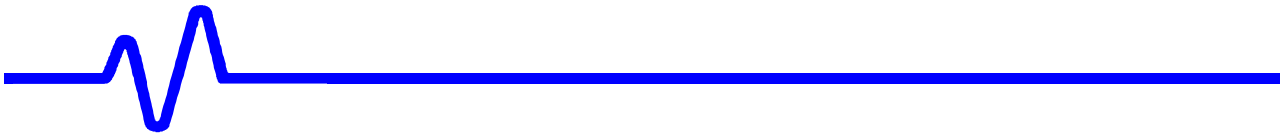
  4) Press **Clear Sweeps**

  5) After 100 sweeps, Read off the **DSO Mean parameter** voltage, and record the measurement in Table 12, column **Mean**.

- Repeat the test for the other channels, substituting channel controls and input connector. Record the measurements in Table 12.
- Set DSO input gain to **5 mv/div** and DSO Offset to **+1 Volt** on all 4 Channels**.**
- Set the output of the external **DC voltage reference source** to **–1 Volt.**
- Repeat steps 1), 2), 3), 4) and 5) on all 4 Channels.
- Record the measurements in Table 12.



- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading.
- Record the test result in Table 12, and compare the **Difference (Δ)** to the corresponding limit in the test record.



b. DC 1MΩ

Procedure

- Recall **LC564D048.PNL** or configure the DSO as shown in 5.8.1.a. and for each Channel make the following change :

  Input Coupling : **DC 1MΩ** on all 4 Channels

  Input gain : **5mV/div** on all 4 Channels

  Input offset : **+1 Volt** on all 4 Channels

- Connect the test equipment as shown in Figure 5-7.

- Set the output of the external **DC voltage reference source** to **–1 Volt**.

  1) Verify that the displayed trace A : Average (1) is on the screen, near the center horizontal graticule line. If the trace is not visible, modify the **DC voltage reference source output** until the trace is within ± 2 divisions of center.

  2) Connect the DMM and record the **voltage reading** in Table 12, column **DMM**.

  3) Disconnect the DMM from the BNC T connector.

  4) Press **Clear Sweeps**

  5) After 100 sweeps, Read off the **DSO Mean parameter** voltage, and record the measurement in Table 12, column **Mean**.

- Repeat the test for the other channels, substituting channel controls and input connector. Record the measurements in Table 12.

- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading.

- Record the test result in Table 12, and compare the **Difference (Δ)** to the corresponding limit in the test record.

5.8.2 Negative Offset Accuracy

a. DC 50Ω

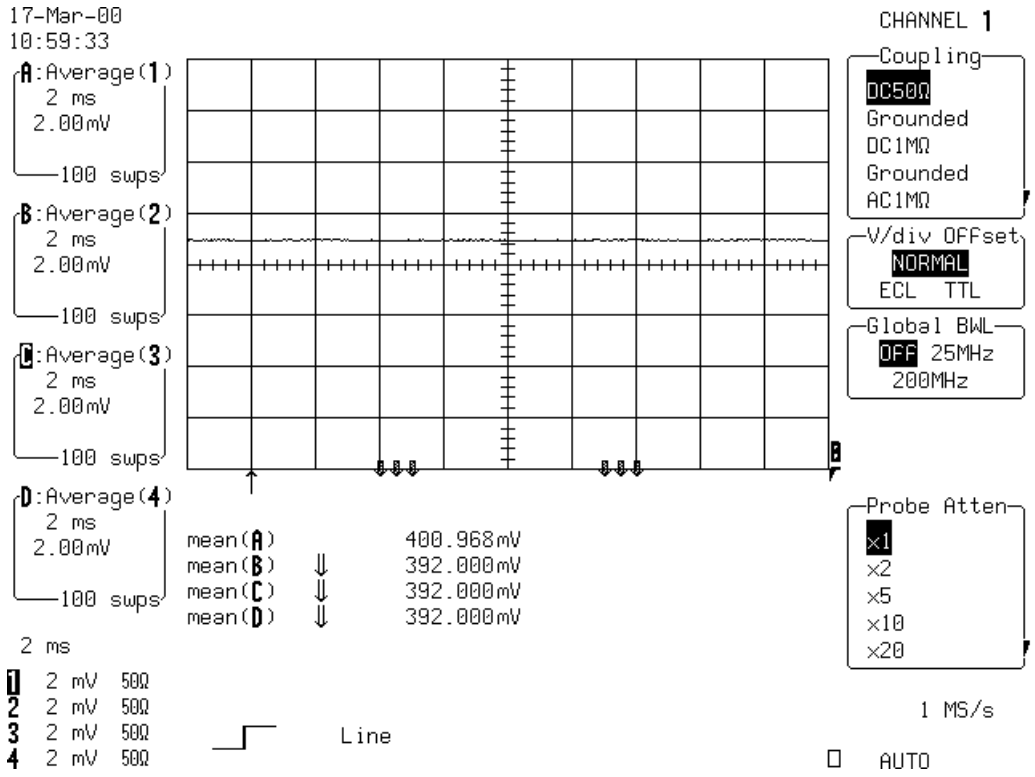
Procedure

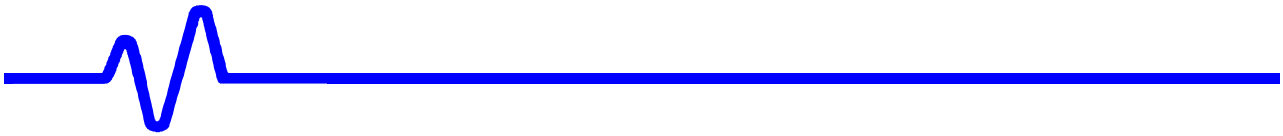
- Recall **LC564D049.PNL** or configure the DSO as shown in 5.8.1.a. and for each Channel make the following change :

  Input offset : **–0.4 Volt** on all 4 Channels

- Connect the test equipment as shown in Figure 5-7.

- Set the output of the external **DC voltage reference source** to **+0.4 Volt.**





1) Verify that the displayed trace A : Average (1) is on the screen, near the center horizontal graticule line. If the trace is not visible, modify the **DC voltage reference source output** until the trace is within ± 2 divisions of center.

2) Connect the DMM and record the **voltage reading** in Table 13, column **DMM**.

3) Disconnect the DMM from the BNC T connector.

4) Press **Clear Sweeps**

5) After 100 sweeps, Read off the **DSO Mean parameter** voltage, and record the measurement in Table 13, column **Mean**.

- Repeat the test for the other channels, substituting channel controls and input connector. Record the measurements in Table 13.
- Set DSO input gain to **5 mv/div** and DSO Offset to **–1 Volt** on all 4 Channels**.**
- Set the output of the external **DC voltage reference source** to **+1 Volt.**
- Repeat steps 1), 2), 3), 4) and 5) on all 4 Channels.
- Record the measurements in Table 13.
- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading. Record the test result in Table 13, and compare the **Difference (Δ)** to the corresponding limit in the test record.

b. DC 1MΩ

- Recall **LC564D050.PNL** or configure the DSO as shown in 5.8.1.a. and for each Channel make the following changes :

Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input Gain	:	**5 mV/div** on all 4 Channels
Input offset	:	**–1 Volt** on all 4 Channels

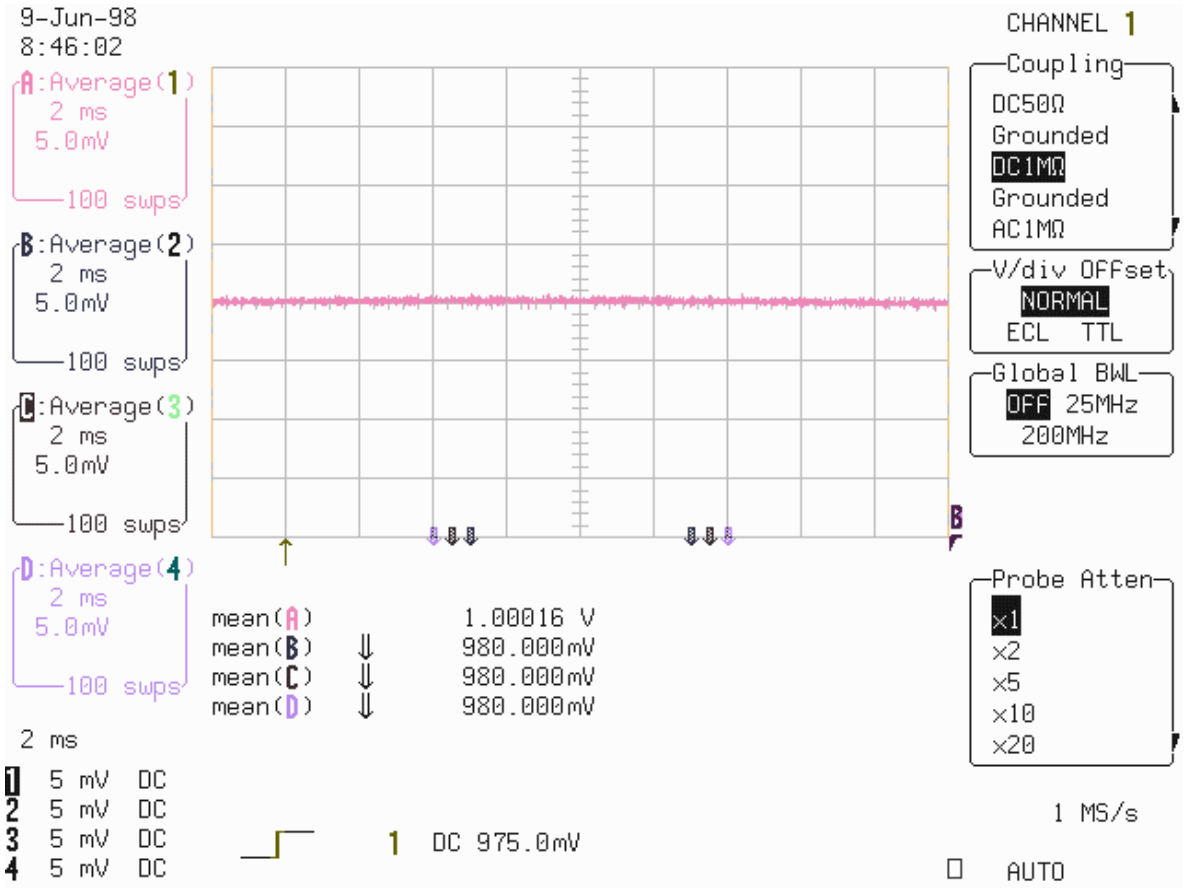
- Connect the test equipment as shown in Figure 5-7.
- Set the output of the external **DC voltage reference source** to **+1 Volt**.

1) Verify that the displayed trace A : Average (1) is on the screen, near the center horizontal graticule line. If the trace is not visible, modify the **DC voltage reference source output** until the trace is within ± 2 divisions of center.
2) Connect the DMM and record the **voltage reading** in Table 13, column **DMM**.

3) Disconnect the DMM from the BNC T connector.

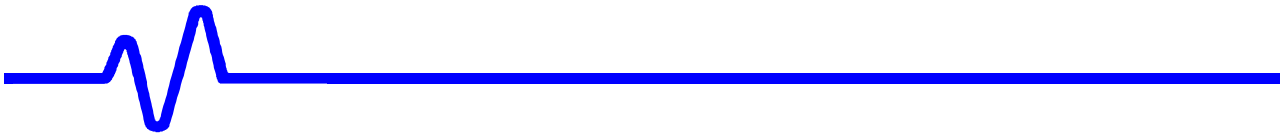
4) Press **Clear Sweeps**

5) After 100 sweeps, Read off the **DSO Mean parameter** voltage, and record the measurement in Table 13, column **Mean**.



- Repeat the test for the other channels, substituting channel controls and input connector. Record the measurements in Table 13.

- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading. Record the test result in Table 13, and compare the **Difference (Δ)** to the corresponding limit in the test record.



5.9 Bandwidth

5.9.1 Description

The purpose of this test is to ensure that the entire system has a bandwidth of at least 1.0 GHz. An external source is used as the reference to provide a signal where amplitude and frequency are well controlled.
The amplitude of the generator as a function of frequency and power is calibrated using an HP8482A sensor on an HP437B power meter or equivalent.

Specifications

50Ω : DC to at least 1.0 GHz (–3 dB) at 10 mV/div. and above.

1MΩ : DC to 500 MHz typical at 100 mV/div.

a. DC 50Ω

- Recall **LC564D051.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 50Ω** on all 4 Channels
Input gain	:	**50 mV/div** on all 4 Channels
Input offset	:	**0 mV** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**Line**
Slope line	:	**Pos**
Mode	:	**Auto**
Time base	:	**1 µsec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
Cursors/Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**On**
Change parameters		
On line 1	:	**Sdev of 1**
On line 2	:	**Sdev of 2**
On line 3	:	**Sdev of 3**
On line 4	:	**Sdev of 4**

- Connect the HP8482A power sensor to the power meter.

- Zero and **calibrate** the HP8482A power sensor using the power meter **Power Ref output**.

- Connect a **BNC adapter** to the HP8482A power sensor.
- Connect a 5ns 50Ω BNC cable to the **RF output** of the HP8648B generator and then through a 6dB attenuator and the necessary adapters to the power sensor.

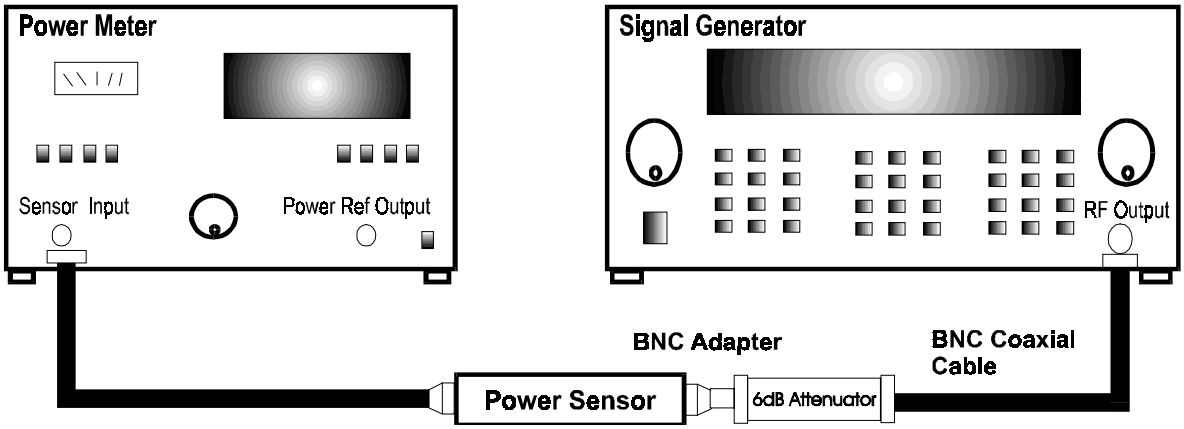


Figure 5-8 : Power Meter Equipment Setup

- Set the generator frequency to **300 kHz**
- Set the generator amplitude to measure **0.200 mW** on the power meter**.**
- Read the displayed **generator output amplitude,** and record it in the third column of Table 14.
- Repeat the above measurement for **1.1 MHz**, **30.1 MHz**, **300.1 MHz**, **700.1 MHz & 1000.1 MHz** Record the generator output amplitude readout in the third column of Table 14.
- Disconnect the **RF output** of the HP8648B generator from the HP8482A power sensor.
- Connect the **RF output** of the HP8648B generator through a 5ns 50 Ohm BNC cable and a 6 dB attenuator into Channel 1.
- Set the generator frequency to **300 kHz**.
- From the generator, apply the **recorded generator signal amplitude** to Channel 1.
- Press **Clear Sweeps**.

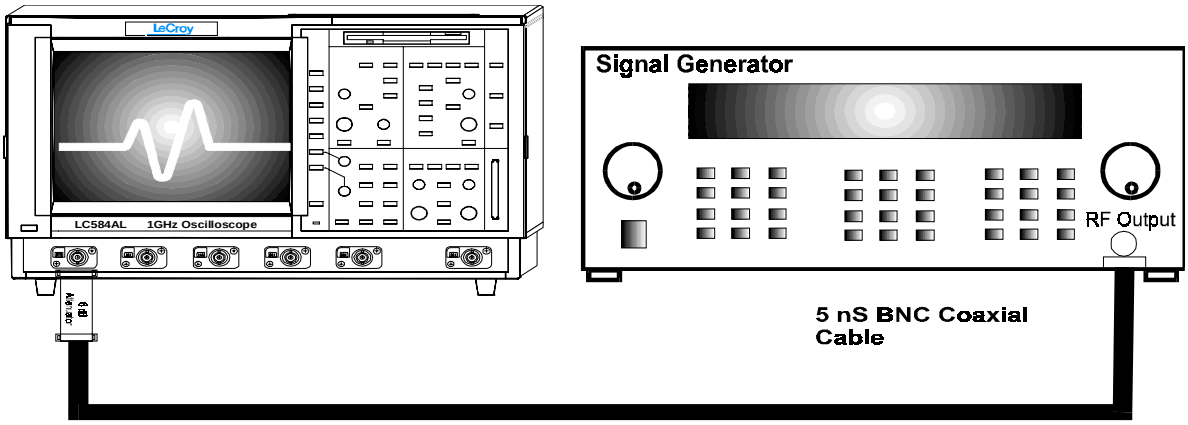
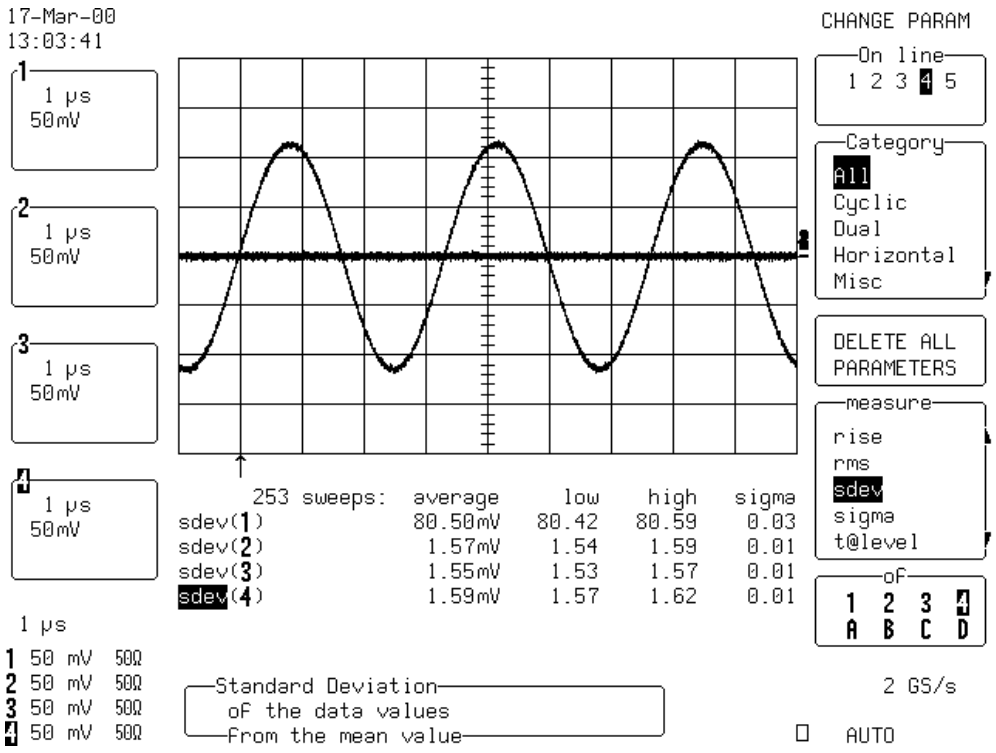


Figure 5-9 : 50Ω Bandwidth Equipment Setup

- Measure for at least 100 sweeps, record the average value of **sdev(1)** inTable14
- Repeat the above 3 steps for Channel 2, Channel 3 & Channel 4 substituting channel controls and input connector. Record the measurements in Table 14.
- Repeat the above measurement for all channels for 1.1 MHz, 30.1 MHz, 300.1 MHz, 700.1 MHz and 1000.1 MHz and record the values in Table 14.
- Calculate the ratio to .3 MHz for each frequency, $sdev_{1.1}/sdev_{0.3}$, $sdev_{30.1}/sdev_{0.3}$ ...$sdev_{1000.1}/sdev_{0.3}$, and compare the results to the limits in the test record.



- Recall **LC564D052.PNL** or configure the DSO as shown in 5.9.1.a. and for each Channel make the following change :

  Input gain : **100mV/div**

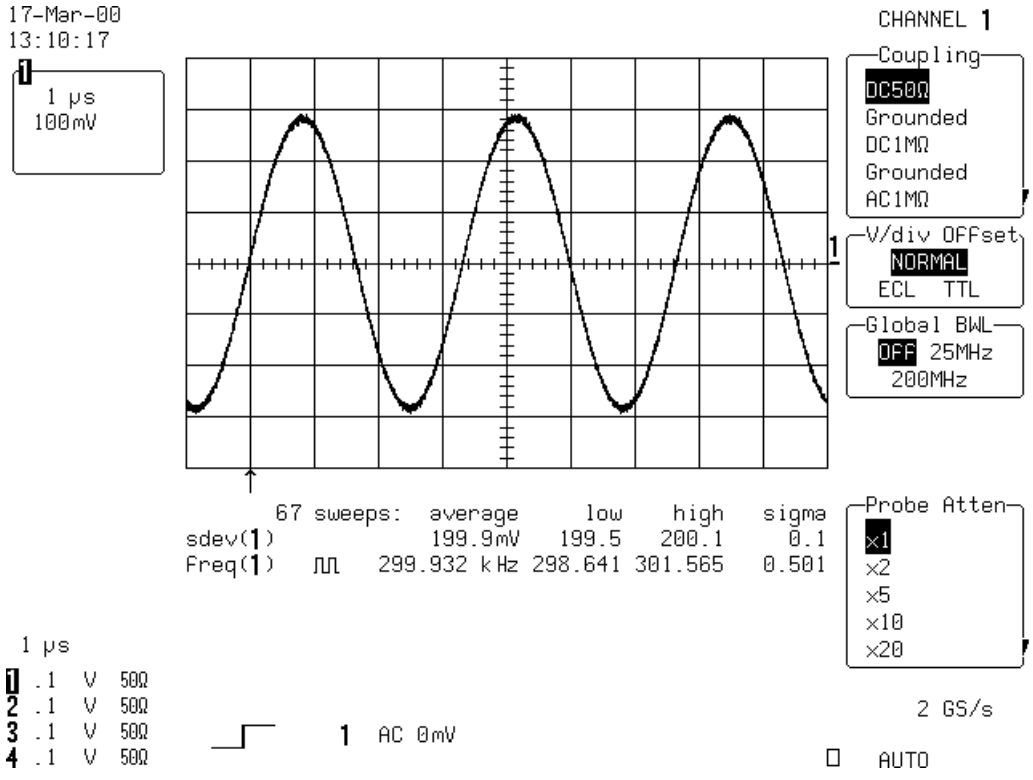
- Connect the test equipment as shown in Figure 5-8.
- Set the generator frequency to **300 kHz**
- Set the generator amplitude to measure **0.800 mW** on the power meter**.**
- Read the displayed **generator output amplitude,** and record it in the third column of Table 15.
- Repeat the above measurement for **1.1 MHz**, **30.1 MHz**, **300.1 MHz**, **700.1 MHz & 1000.1 MHz.** Record the generator output amplitude readout in the third column of Table 15.
- Disconnect the **RF output** of the HP8648B generator from the HP8482A power sensor.
- Connect the test equipment as shown in Figure 5-9.
- Set the generator frequency to **300 kHz**.
- From the generator, apply the **recorded generator signal amplitude** to Channel 1.
- Press **Clear Sweeps**.
- Measure for at least 100 sweeps, record the average value of **sdev(1)** inTable15
- Repeat the above 3 steps for Channel 2, Channel 3 & Channel 4 substituting channel controls and input connector. Record the measurements in Table 15.
- Repeat the above measurement for all channels for 1.1 MHz, 30.1 MHz, 300.1 MHz, 700.1 MHz & 1000.1 MHz and record the values in Table 15.
- Calculate the ratio to .3 MHz for each frequency, $sdev_{1.1}/sdev_{0.3}$, $sdev_{30.1}/sdev_{0.3}$ ...$sdev_{1000.1}/sdev_{0.3}$, and compare the results to the limits in the test record.

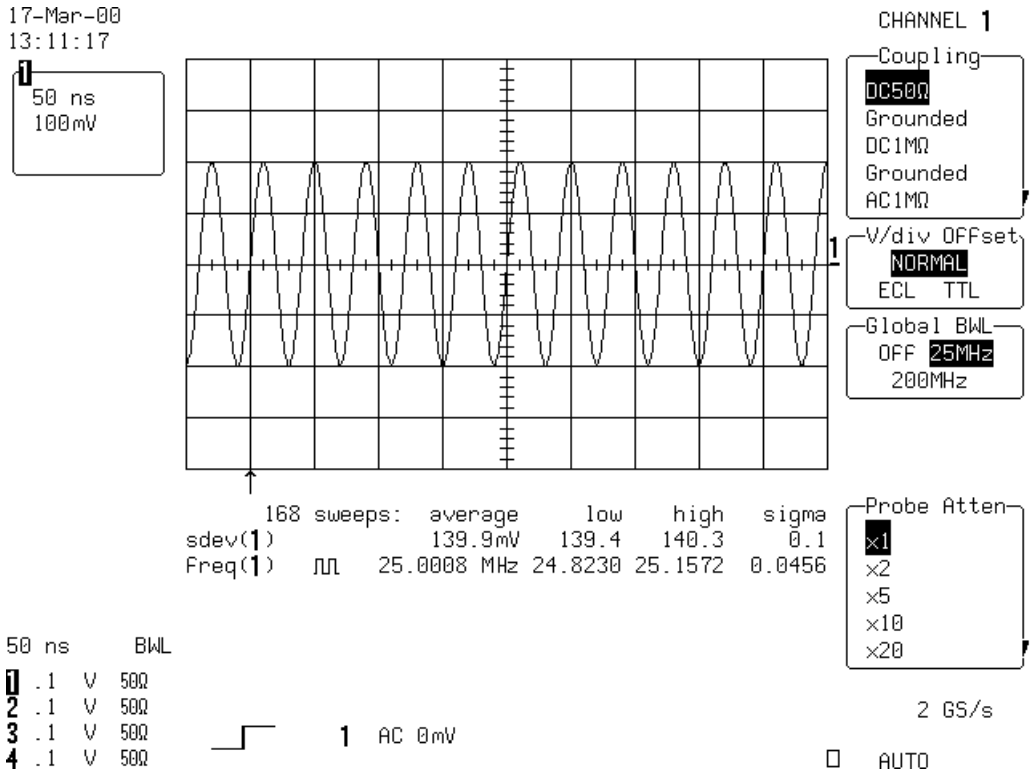
b. DC 50Ω with Bandwidth Limiter On

- Recall **LC564D053.PNL** or configure the DSO

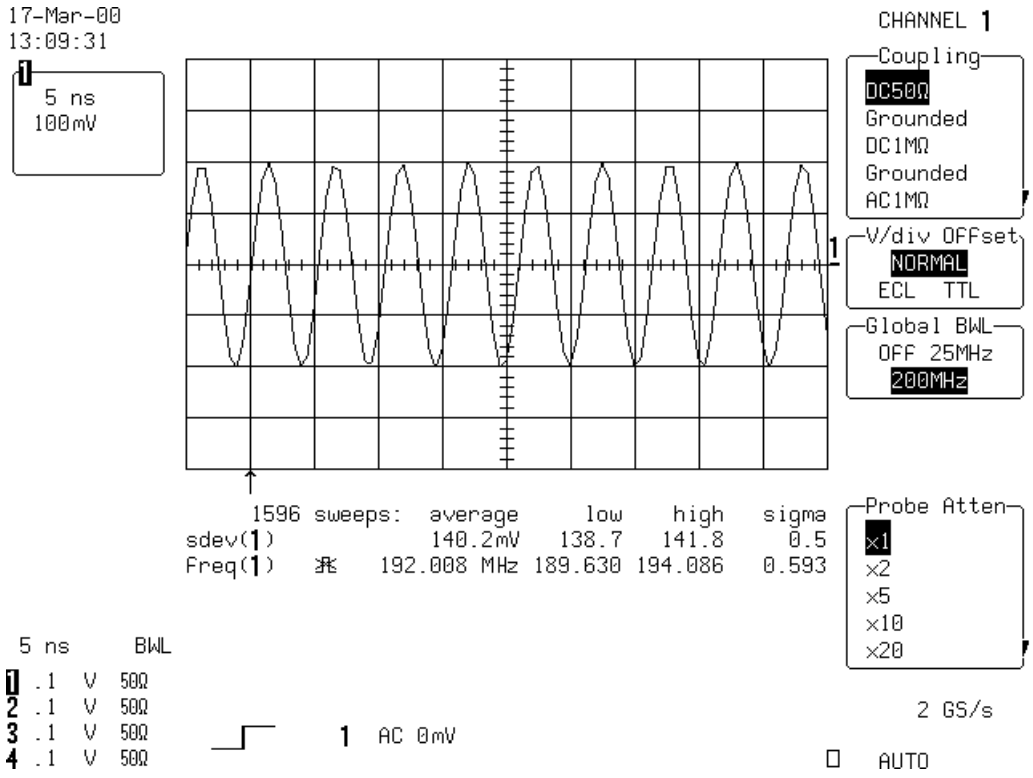
Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1**
Input Coupling	:	**DC 50Ω**
Global BWL	:	**25 MHz**
Input gain	:	**100 mV/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**1**
Slope line	:	**Pos**
Mode	:	**Auto**
Time base	:	**1 µsec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
Cursors/Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**Off**
Change parameters		
On line 1	:	**Sdev of 1**
On line 2	:	**Freq of 1**

- Connect the test equipment as shown in Figure 5-9.
- Set the generator frequency to **300 kHz**.
- Adjust the generator signal amplitude to measure **sdev(1)** = **200 mV.**
- Set Time base : **50 nsec/div**.
- Increase the generator frequency until **sdev(1)** = **140 mV.** (typically 25 MHz)
- Press **Clear Sweeps**
- When **sdev(1)** = **140 mV,** record Freq(1) in Table 16.
- Check that the frequency is within the limits specified in Table 16.


17-Mar-00
13:10:17
1 µs
100mV
CHANNEL 1
Coupling
DC50Ω
Grounded
DC1MΩ
Grounded
AC1MΩ
V/div OFFset
NORMAL
ECL TTL
Global BWL
OFF 25MHz
200MHz
67 sweeps: average low high sigma
sdev(1) 199.9mV 199.5 200.1 0.1
Freq(1) 299.932 kHz 298.641 301.565 0.501
Probe Atten
×1
×2
×5
×10
×20
1 µs
1 .1 V 50Ω
2 .1 V 50Ω
3 .1 V 50Ω
4 .1 V 50Ω
1 AC 0mV
2 GS/s
AUTO


17-Mar-00
13:11:17
50 ns
100mV
CHANNEL 1
Coupling
DC50Ω
Grounded
DC1MΩ
Grounded
AC1MΩ
V/div OFFset
NORMAL
ECL TTL
Global BWL
OFF 25MHz
200MHz
168 sweeps: average low high sigma
sdev(1) 139.9mV 139.4 140.3 0.1
Freq(1) 25.0008 MHz 24.8230 25.1572 0.0456
Probe Atten
×1
×2
×5
×10
×20
50 ns BWL
1 .1 V 50Ω
2 .1 V 50Ω
3 .1 V 50Ω
4 .1 V 50Ω
1 AC 0mV
2 GS/s
AUTO

- Set Global BWL : **200 MHz**
- Set Timebase : **5 nsec/div**.
- Increase the generator frequency until **sdev(1)** = **140 mV.** (typically 200 MHz)



- Press **Clear Sweeps**
- When **sdev(1)** = **140 mV,** record Freq(1) in Table 16.
- Repeat the 25 MHz and 200 MHz Bandwidth limiter tests for the other channels, substituting channel controls and input connector.
- Recall **LC564D054.PNL** for Channel 2**, LC564D055.PNL** for Channel3 **LC564D056.PNL** for Channel 4, or configure the DSO as shown in 5.9.1.b. and make the necessary changes.
- Record the test results in Table 16, and compare the results to the limits.

5.9.2 DC 1MΩ

- Recall **LC564D057.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	**100 mV/div.** on all 4 Channels
Input offset	:	**0 mV** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**Line**
Slope line	:	**Pos**
Mode	:	**Auto**
Time base	:	**1 µsec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
Cursors/Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**On**
Change parameters		
On line 1	:	**Sdev of 1**
On line 2	:	**Sdev of 2**
On line 3	:	**Sdev of 3**
On line 4	:	**Sdev of 4**

- Connect the test equipment as shown in Figure 5-10.

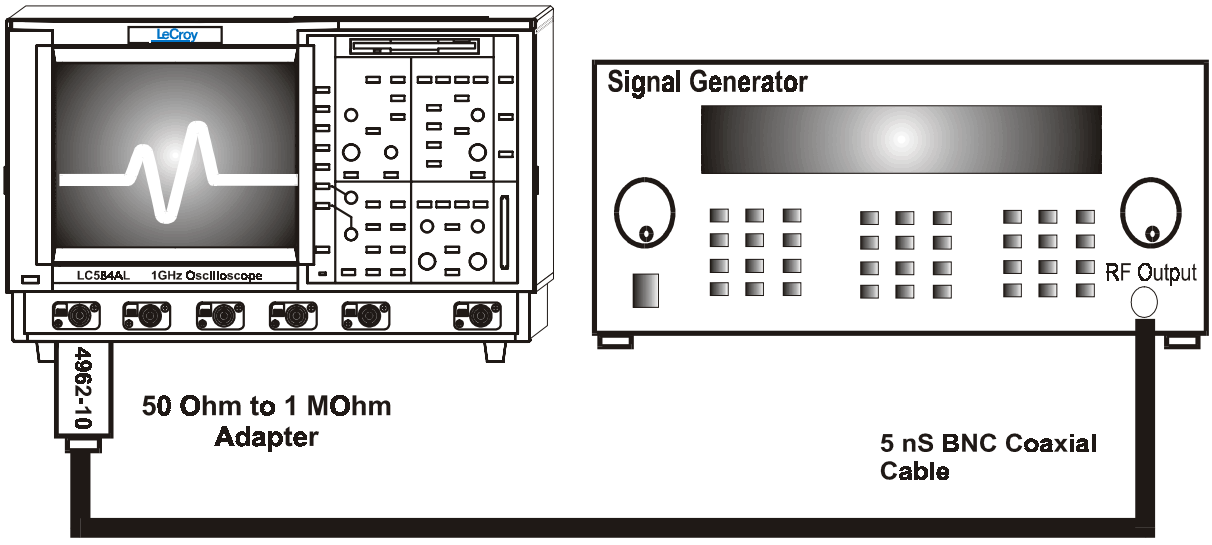
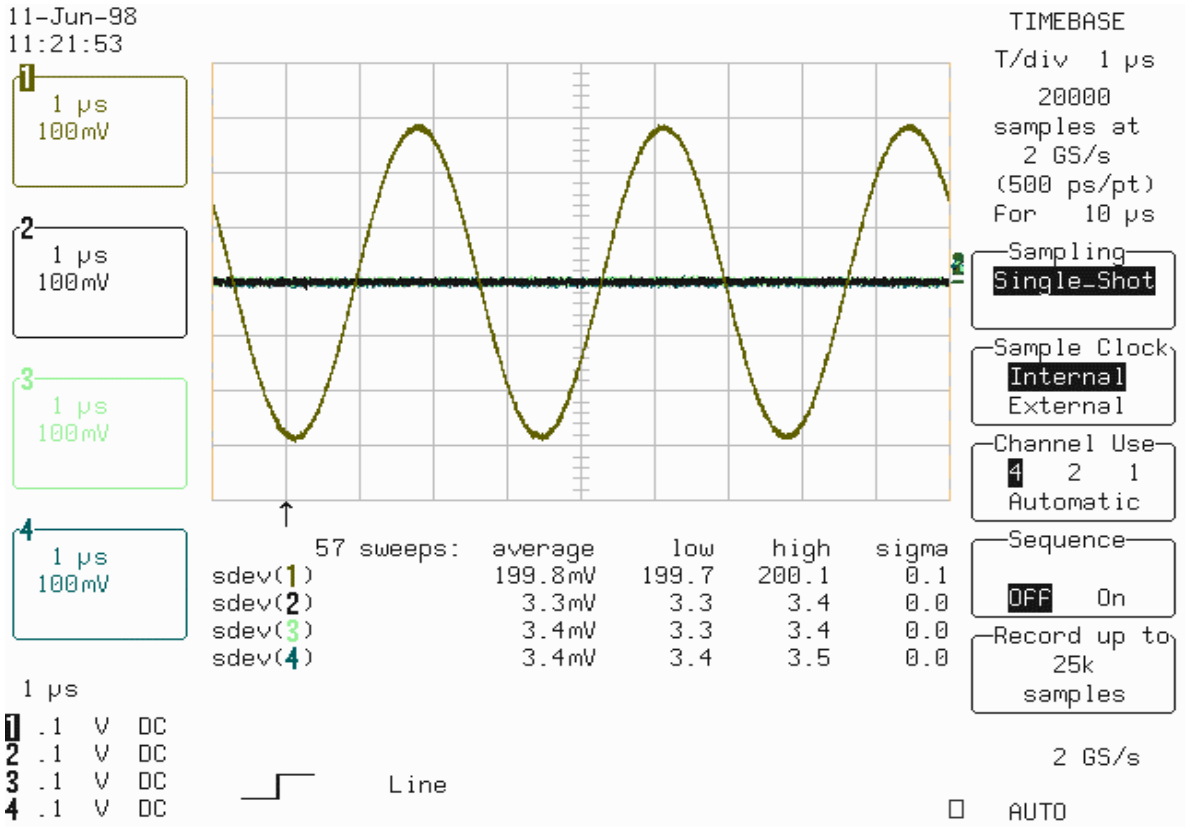


Figure 5-10 : 1MΩ Bandwidth Equipment Setup

- Set the generator frequency to **300 kHz**.

- Adjust the generator signal amplitude to measure **sdev(1)** = **200 mV.**



- Disconnect the coaxial cable from the 4962-10 adapter. Connect the test equipment as shown in Figure 5-11.

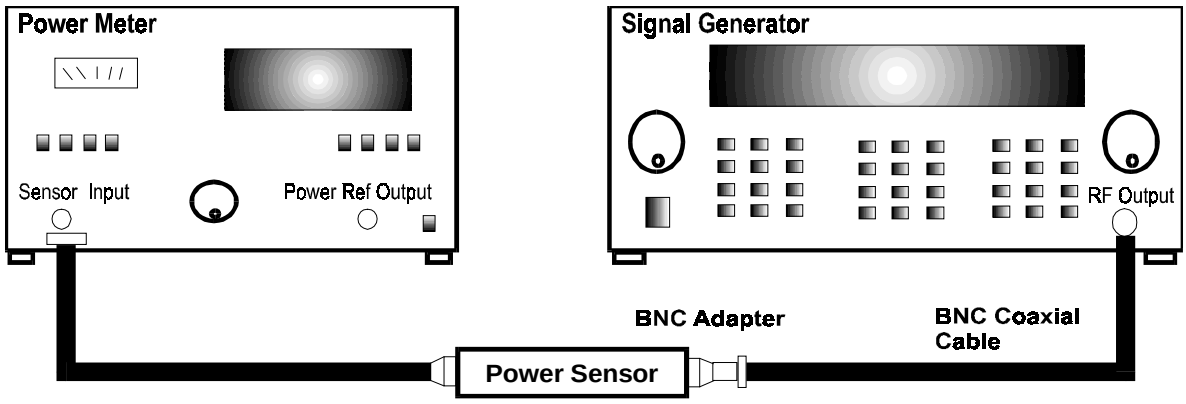
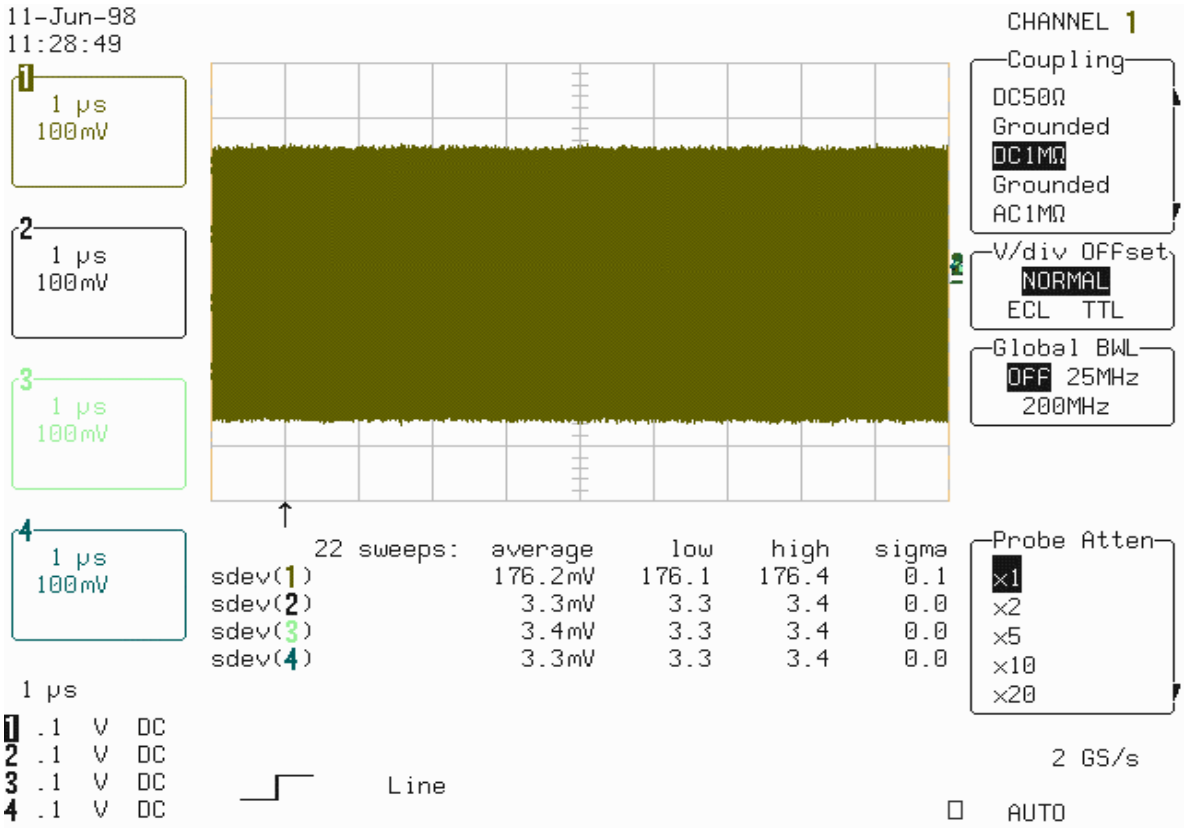
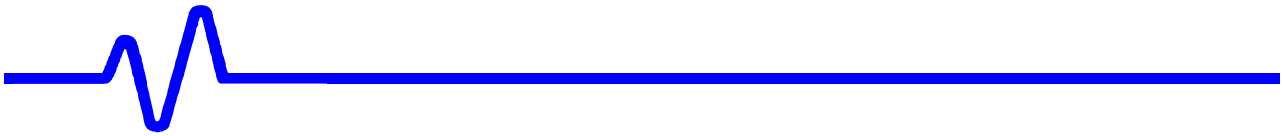


Figure 5-11 : Power Meter Equipment Setup

- Record the displayed power meter value in mW.
- Set the generator frequency to **500.1 MHz**.
- Now fine adjust the generator amplitude output until the power meter readout indicates the value measured just above at 300 kHz.
- Reconnect the signal generator to DSO Channel 1, as shown in Figure 5-10.
- Press **Clear Sweeps**.
- Measure for at least **100 sweeps**, record the average value of **sdev(1)** in Table 17.
- Repeat the above steps for Channel 2, Channel 3 & Channel 4, substituting channel controls and input connector.
- Record the sdev measurements in Table 17.
- Calculate the ratio $\mathbf{sdev_{500.1}/sdev_{0.3}}$ for each Channel, and test each value against the limits shown in the test record.





5.10 Trigger Level

5.10.1 Description

The trigger capabilities are tested for several cases of the standard edge trigger:

- Channel (internal), and External Trigger sources
- Three levels: –3, 0, +3 major screen divisions
- DC coupling
- Positive and negative slopes

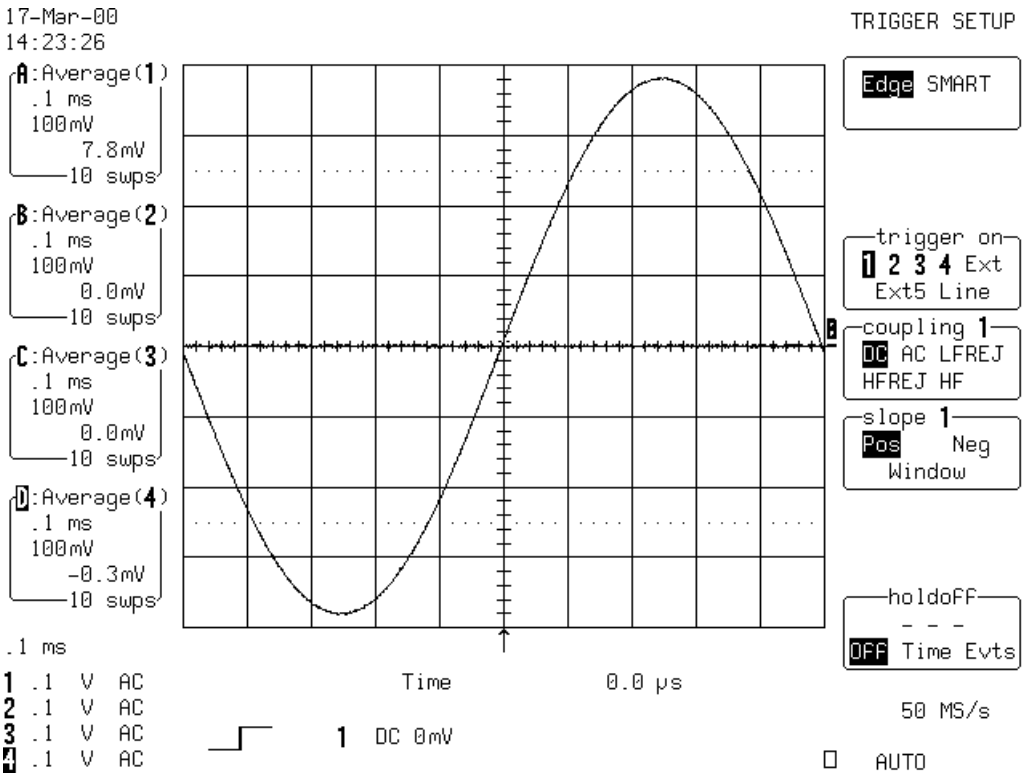
5.10.2 Channel Trigger at 0 Division Threshold

DC Coupling

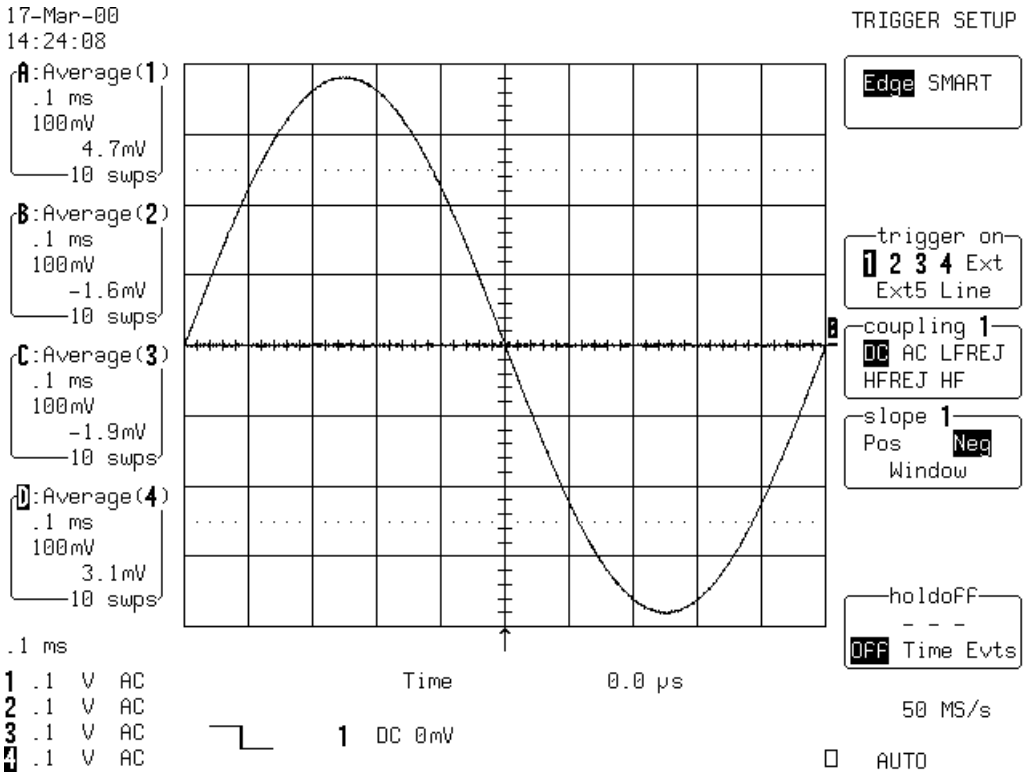
Recall **LC564D058.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 50Ω** on all 4 Channels
Input gain	:	**100 mV/div.** on all 4 Channels
Input offset	:	**0 mV** on all 4 Channels (use show status to verify)
Trigger setup	:	**Edge**
Trigger on	:	**1**
Slope 1	:	**Pos**
Coupling	:	**DC**
Mode	:	**Auto**
Set Trigger level	:	**DC 0.0 mV**
Pre-Trigger Delay	:	**50 %**
Time base	:	**0.1 msec/div.**
Record up to	:	**50 k samples**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
Zoom+Math Trace ON		**A, B, C & D**
Select Math Setup		
For Math	:	**Use at most 5000 points**
Redefine A, B, C, D		**Channel 1, Channel 2, Channel 3 & Channel 4**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**10 sweeps**

- Set the output of the LeCroy LW420 or equivalent audio frequency signal generator to **1 kHz.**
- Connect the output of the generator to Channel 1 through a 50 Ohm coaxial cable and adjust the sine wave output amplitude to get **8 divisions peak to peak.**
- Select Cursors/Measure: **Cursors, Time, Absolute**
- Use the "cursor position" knob, to move the **Time marker** at 0.0 µs



- Press **Clear Sweeps**,
- Acquire 10 sweeps and record in Table 18 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**
- Compare the test results to the corresponding limit in the test record.
- Set Trigger Slope 1 : **Neg**
- Acquire 10 sweeps and record in Table 18 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**



- Repeat these steps for all input channels, substituting channel controls (DC, Pos, Neg) and input connector.
  Recall **L564D059.PNL** for Channel 2, **L564D0060.PNL** for Channel 3, **L564D061.PNL** for Channel 4, or select **Trigger on** the Channel under test.
  The **Trigger level** is displayed in either the icon **2**, **3** or **4**

- Record the measurements in Table 18 and compare the test results to the corresponding limits in the test record.

5.10.3 Channel Trigger at +3 Divisions Threshold

DC Coupling

- Recall **LC564D062.PNL** or configure the DSO as shown in 5.10.2.a and for each Channel make the following change :

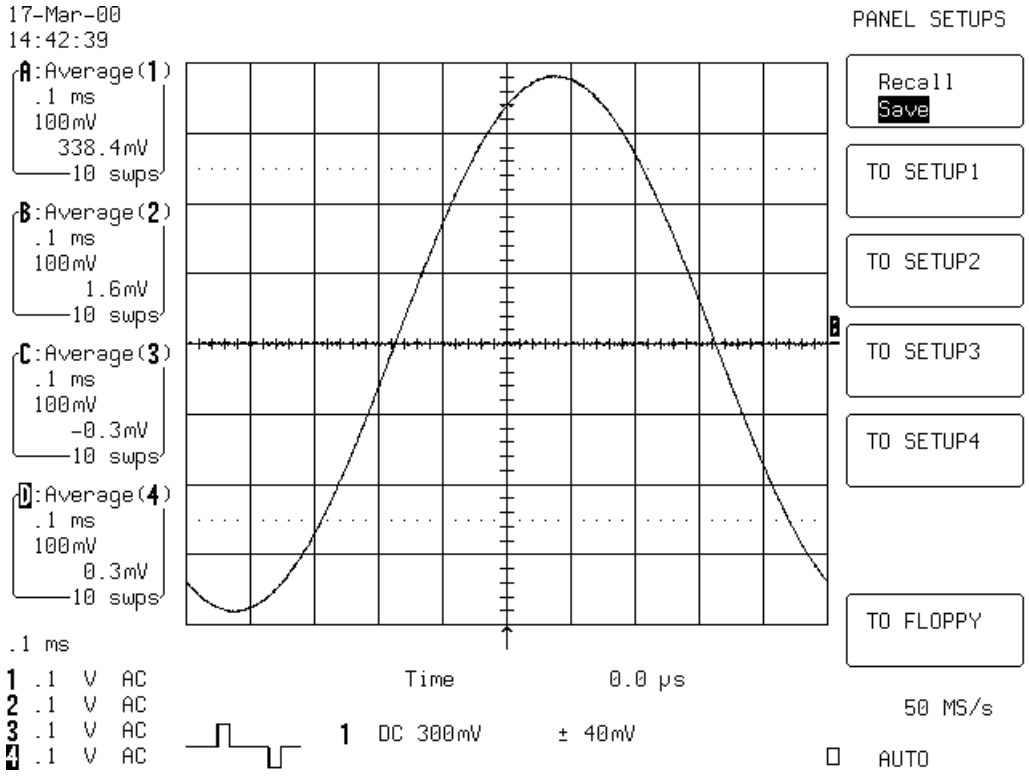
  Set Trigger level : **DC +300 mV**

- Connect the output of the generator to Channel 1 through a 50 Ohm coaxial cable.

- Press **Clear Sweeps**,

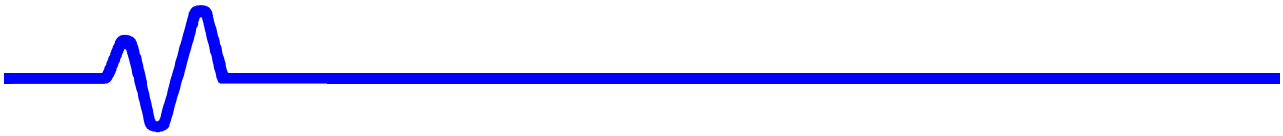
- Acquire 10 sweeps and record in Table 18 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**

- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope 1 : **Neg**

- Acquire 10 sweeps and record in Table 18 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**



- Repeat these steps for all input channels, substituting channel controls (DC, Pos, Neg) and input connector.
  Recall **L564D063.PNL** for Channel 2, **L564D064.PNL** for Channel 3, **L564D065.PNL** for Channel 4, or select **Trigger on** the Channel under test. The **Trigger level** is displayed in either the icon **2**, **3** or **4**

- Record the measurements in Table 18 and compare the test results to the corresponding limits in the test record.

5.10.4 Channel Trigger at –3 Divisions Threshold

DC Coupling

- Recall **LC564D066.PNL** or configure the DSO as shown in 5.10.2.a and for each channel make the following change :

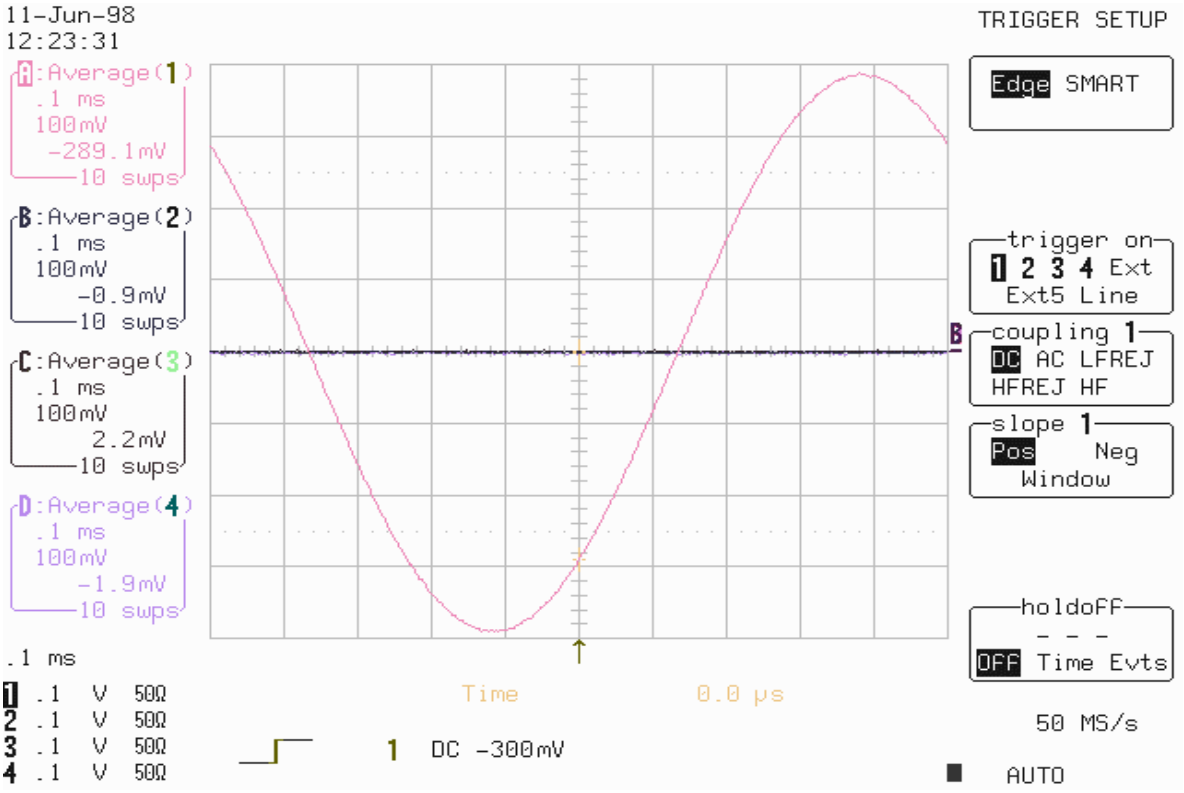
  Set Trigger level：**DC –300 mV**

- Connect the output of the generator to Channel 1 through a 50 Ohm coaxial cable.

- Press **Clear Sweeps**,

- Acquire 10 sweeps and record in Table 18 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**

- Compare the test results to the corresponding limit in the test record.

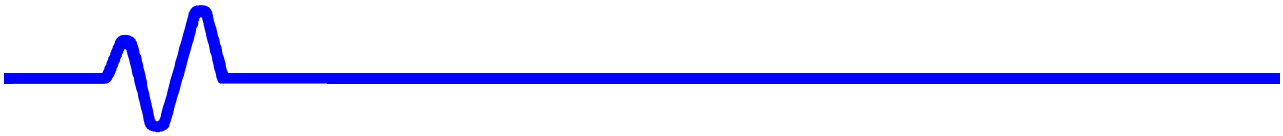


- Set Trigger Slope 1 : **Neg**

- Acquire 10 sweeps and record in Table 18 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**

- Repeat these steps for all input channels, substituting channel controls (DC, Pos, Neg) and input connector.
  Recall **L564D067.PNL** for Channel 2, **L564D068.PNL** for Channel 3, **L564D069.PNL** for Channel 4, or select **Trigger on** the Channel under test.
  The **Trigger level** is displayed in either the icon **2**, **3** or **4**

- Record the measurements in Table 18 and compare the test results to the corresponding limits in the test record.



5.10.5 External Trigger at 0 Division Threshold

DC Coupling

- Recall **LC564D070.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channel Trace ON		**Channel 2**
Input Coupling	:	**DC 50Ω**
Input gain	:	**100 mV/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**Ext**
Slope Ext	:	**Pos**
Coupling Ext	:	**DC**
Set Trigger level	:	**0.0 mV**
External	:	**DC 1MΩ**
Mode	:	**Auto**
Pre-Trigger Delay	:	**50 %**
Time base	:	**0.1 msec/div.**
Record up to	:	**50 k samples**
Channel Trace OFF		**Channel 2**
Zoom+Math Trace ON		**B**
Select Math Setup		
For Math	:	**Use at most 5000 points**
Redefine B	:	**Channel 2**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**10 sweeps**

- Connect the test equipment as shown in Figure 5-12.
- Set the output of the LeCroy LW420 or equivalent audio frequency signal generator to **1 kHz.**
- Adjust the sine wave output amplitude to get **8 divisions peak to peak .**
- Select Cursors/Measure : **Cursors, Time, Absolute**
- Use the "cursor position" knob, to move the **Time marker** at 0.0 µs

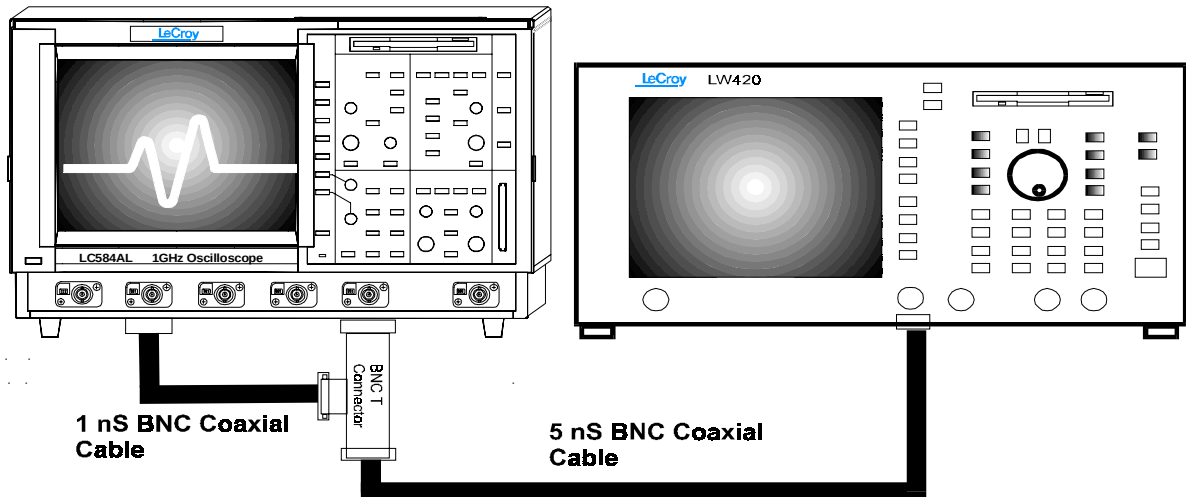
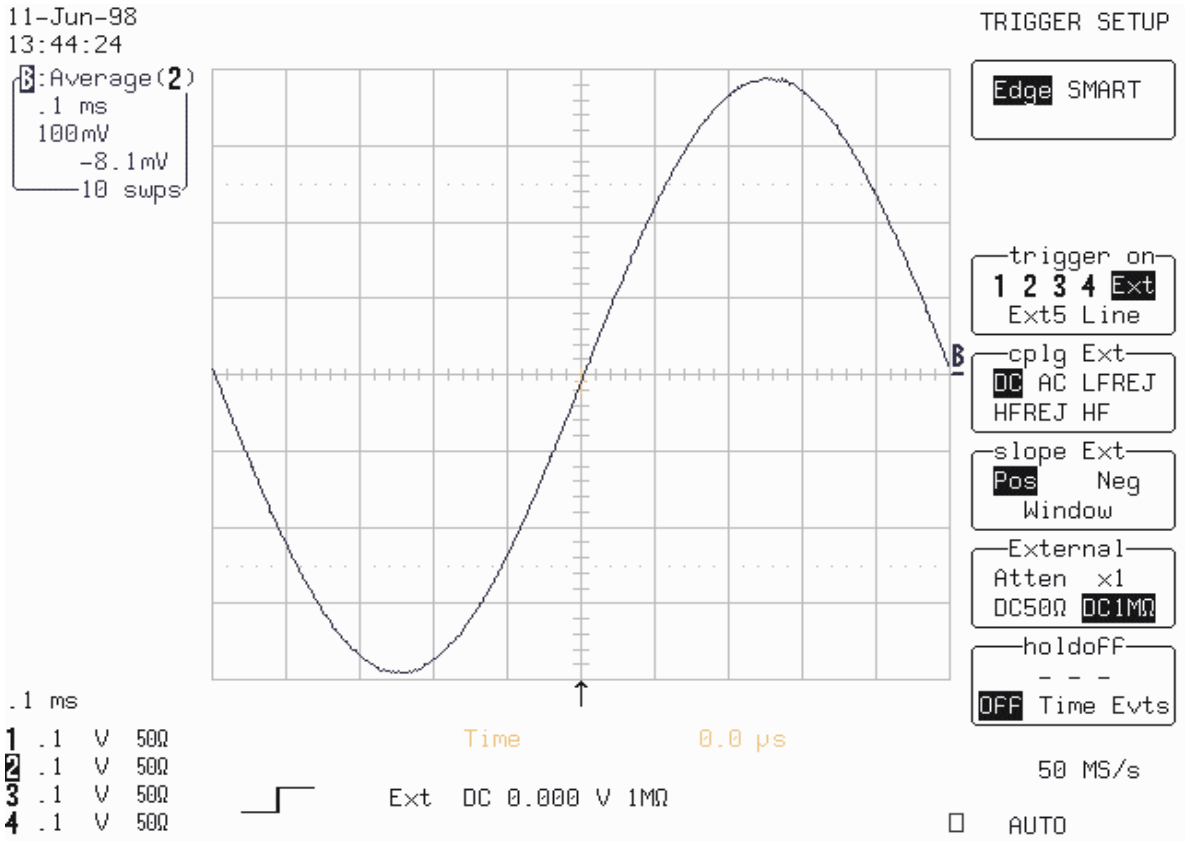


Figure 5-12 : External Trigger Equipment Setup

- Press **Clear Sweeps**
- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**



- Set Trigger Slope Ext : **Neg**
- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.

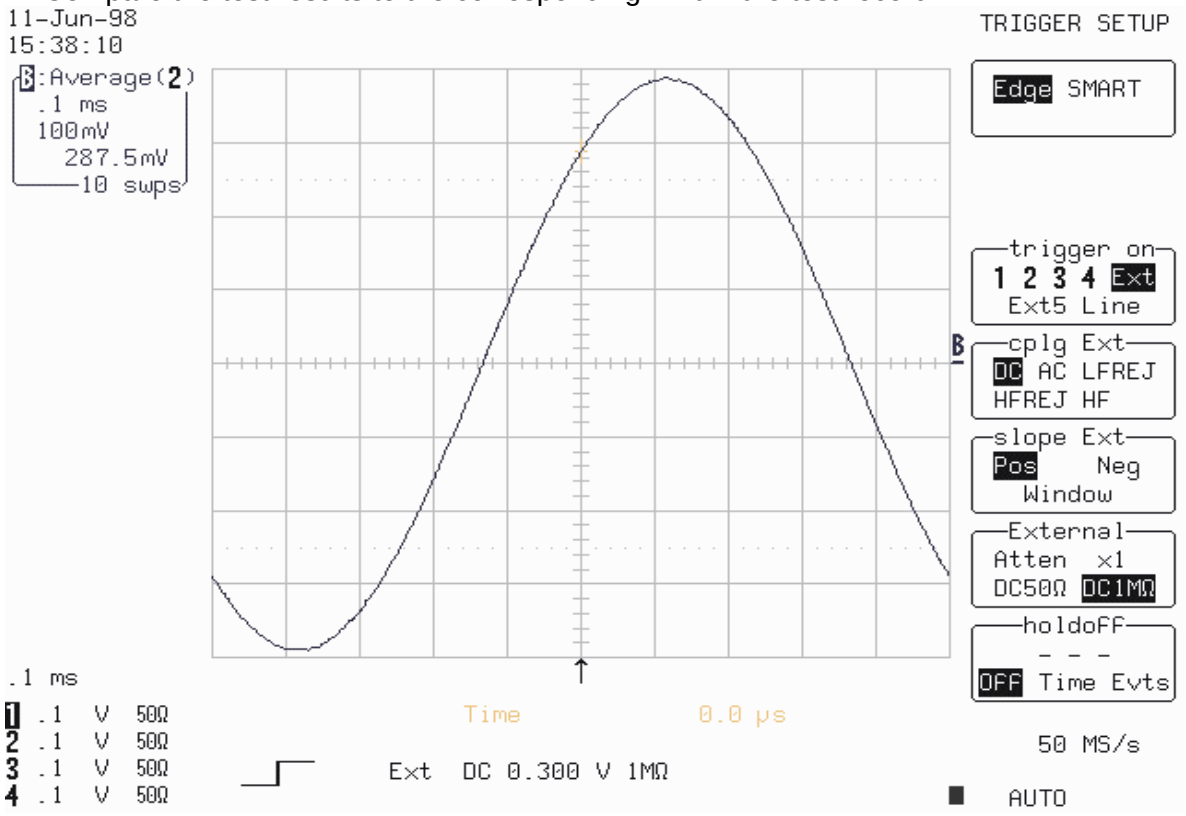
5.10.6 External Trigger at +3 Divisions Threshold

DC Coupling

- Recall **LC564D071.PNL** or configure the DSO as shown in 5.10.5.a and make the following change :

  Set Ext Trigger level : **DC +300 mV**

- Connect the test equipment as shown in Figure 5-12.
- Press **Clear Sweeps**,
- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope Ext : **Neg**

- Acquire 10 sweeps and record in Table 21 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

5.10.7 External Trigger at –3 Divisions Threshold

DC Coupling

- Recall **LC564D072.PNL** or configure the DSO as shown in 5.10.5.a and make the following change :

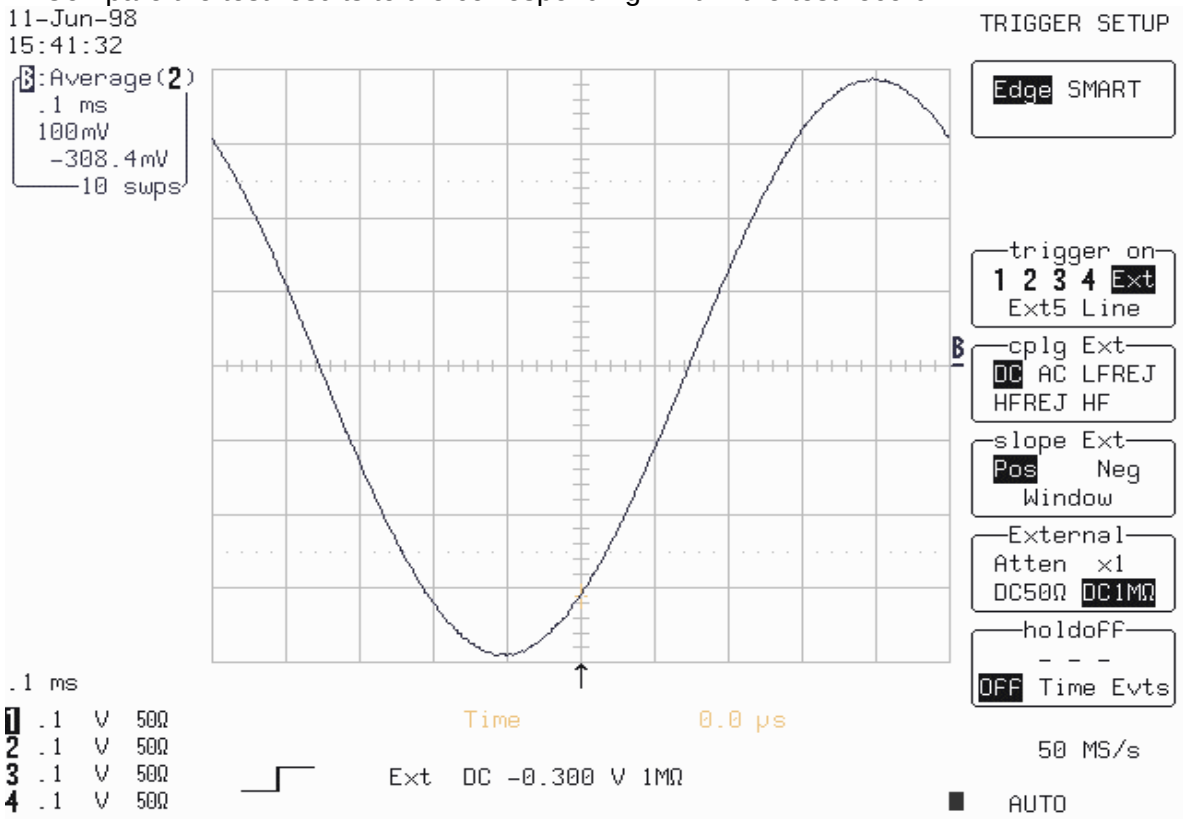
  Set Ext Trigger level : **DC –300 mV**

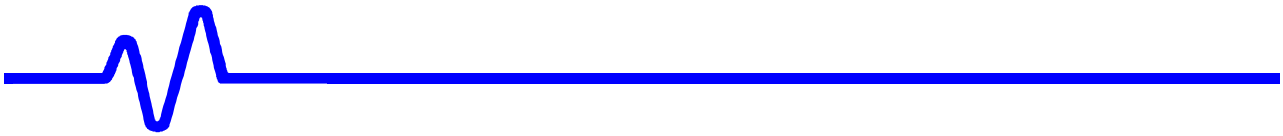
- Connect the test equipment as shown in Figure 5-12.

- Press **Clear Sweeps**.

- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

- Compare the test results to the corresponding limit in the test record.





- Set Trigger Slope Ext : **Neg**

- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

5.10.8 External/5 Trigger at 0 Division Threshold

DC Coupling

- Recall **LC564D073.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channel Trace ON		**Channel 2**
Input Coupling	:	**DC 1MΩ**
Input gain	:	**1V/div**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**Ext5**
Slope Ext/5	:	**Pos**
Mode	:	**Auto**
Coupling	:	**DC**
Set Trigger level	:	**0.0 mV**
External	:	**DC 1MΩ**
Pre-Trigger Delay	:	**50 %**
Time base	:	**0.1 msec/div.**
Record up to	:	**50 k samples**
Channel Trace OFF		**Channel 2**
Zoom+Math Trace ON		**B**
Select Math Setup		
For Math	:	**Use at most 5000 points**
Redefine B	:	**Channel 2**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**10 sweeps**

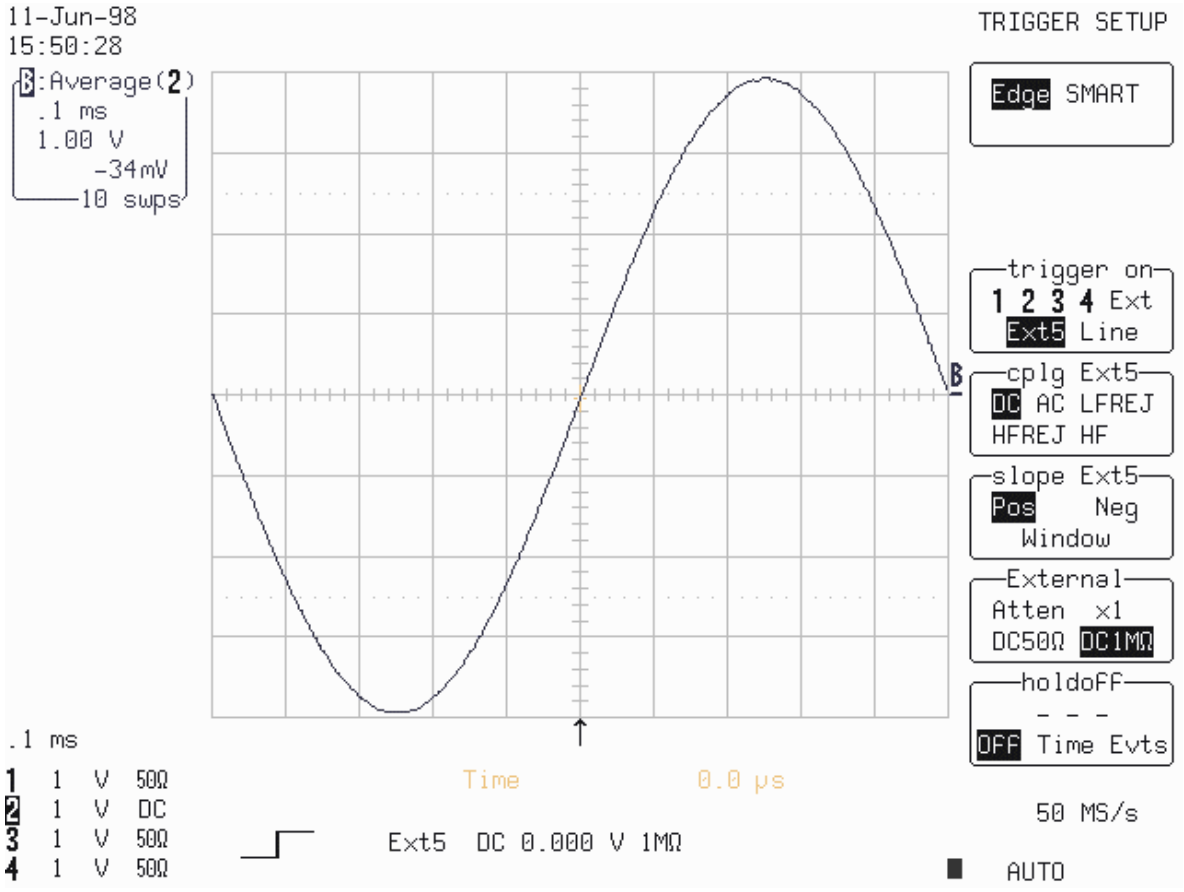
- Connect the test equipment as shown in Figure 5-12.

- Set the output of the LeCroy LW420 or equivalent audio frequency signal generator to **1 kHz.**

- Adjust the sine wave output amplitude to get **8 divisions peak to peak .**

- Select Cursors/Measure : **Cursors, Time, Absolute**

- Use the "cursor position" knob, to move the **Time marker** at 0.0 µs
- Press **Clear Sweeps**
- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**



- Set Trigger Slope Ext5 : **Neg**
- Acquire 10 sweeps and record in Table 21 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.

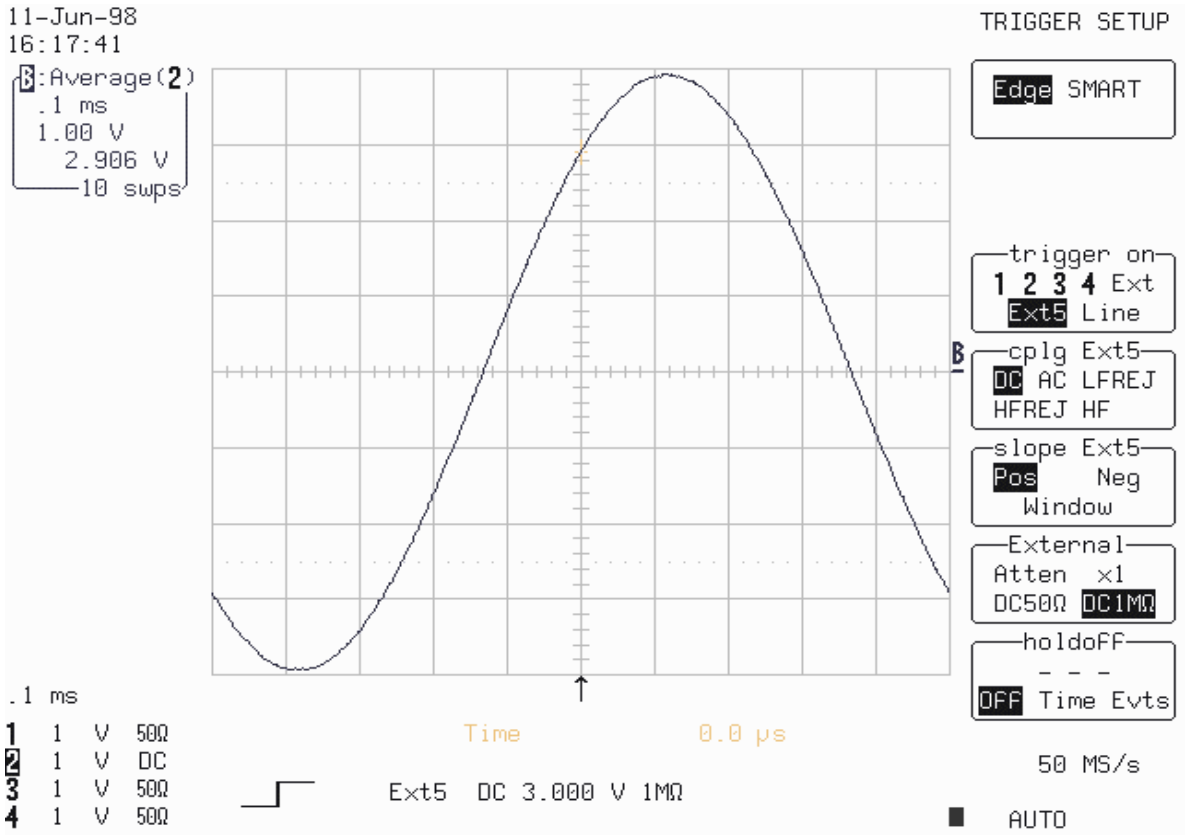
5.10.9 External/5 Trigger at +3 Divisions Threshold

DC Coupling

- Recall **LC564D074.PNL** or configure the DSO as shown in 5.10.8.a and make the following change :

  Set Ext/5 Trigger level : **DC +3 V**

- Connect the test equipment as shown in Figure 5-12.
- Press **Clear Sweeps**,
- Acquire 10 sweeps and record in Table 21 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope Ext/5 : **Neg**
- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

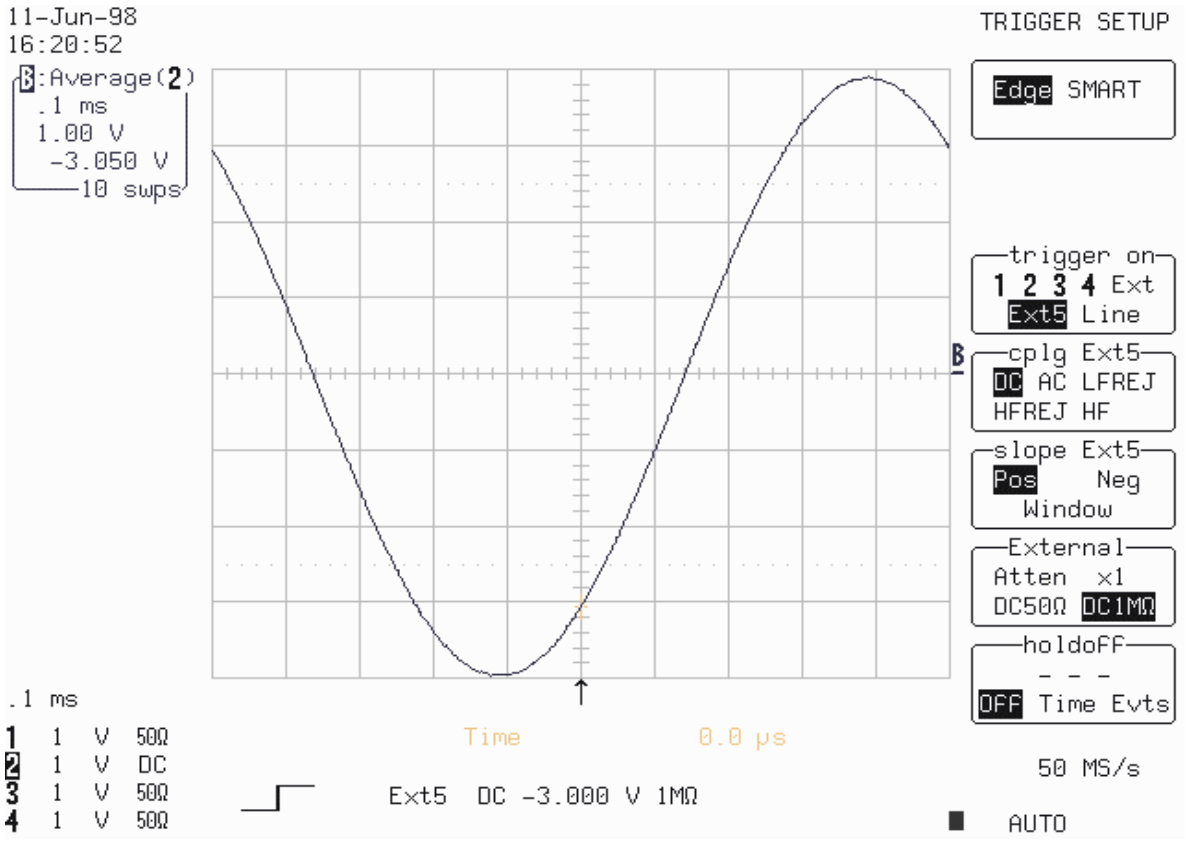
5.10.10 External/5 Trigger at –3 Divisions Threshold

DC Coupling

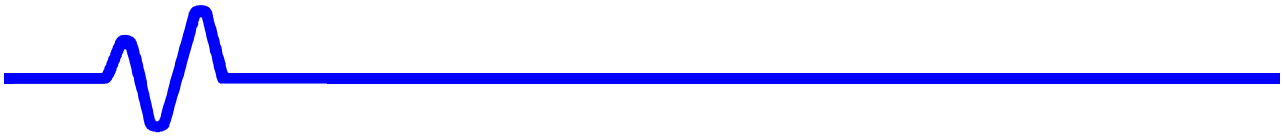
- Recall **LC564D075.PNL** or configure the DSO as shown in 5.10.5.a and make the following change :

  Set Ext/5 Trigger level : **DC –3 V**

- Connect the test equipment as shown in Figure 5-12.
- Press **Clear Sweeps**.
- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope Ext/5 : **Neg**
- Acquire 10 sweeps and record in Table 19 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**



5.11 Smart Trigger

5.11.1 Trigger on Pulse Width 10 nsec

a. Pulse Width < 10 nsec

- Recall **LC564D076.PNL** or configure the DSO

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels trace ON		**Channel 1**
Input coupling	:	**DC 50Ω**
Input gain	:	**.5 V/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Smart**
Setup Smart Trigger		**Glitch**
Trigger on	:	**1**
At the end of	:	**Neg.**
Width < 10 nsec	:	**On**
Width > 10 nsec	:	**Off**
Trigger mode	:	**Norm**
Time base	:	**5 nsec/div.**

- Connect the **RF output** of the HP8648B generator through a 5ns 50 Ohm BNC coaxial cable into Channel 1.

- Set the generator frequency to **100 MHz**. Adjust the generator output amplitude to get **5 divisions peak to peak .**

- Check that the scope Triggers. Record the test result in Table 20.

- Set Width < 10 nsec **Off** and Width > 10 nsec **ON**

- Check that the scope **doesn't trigger :** slow trigger and no flashes in box next to normal. Record the test result in Table 20.

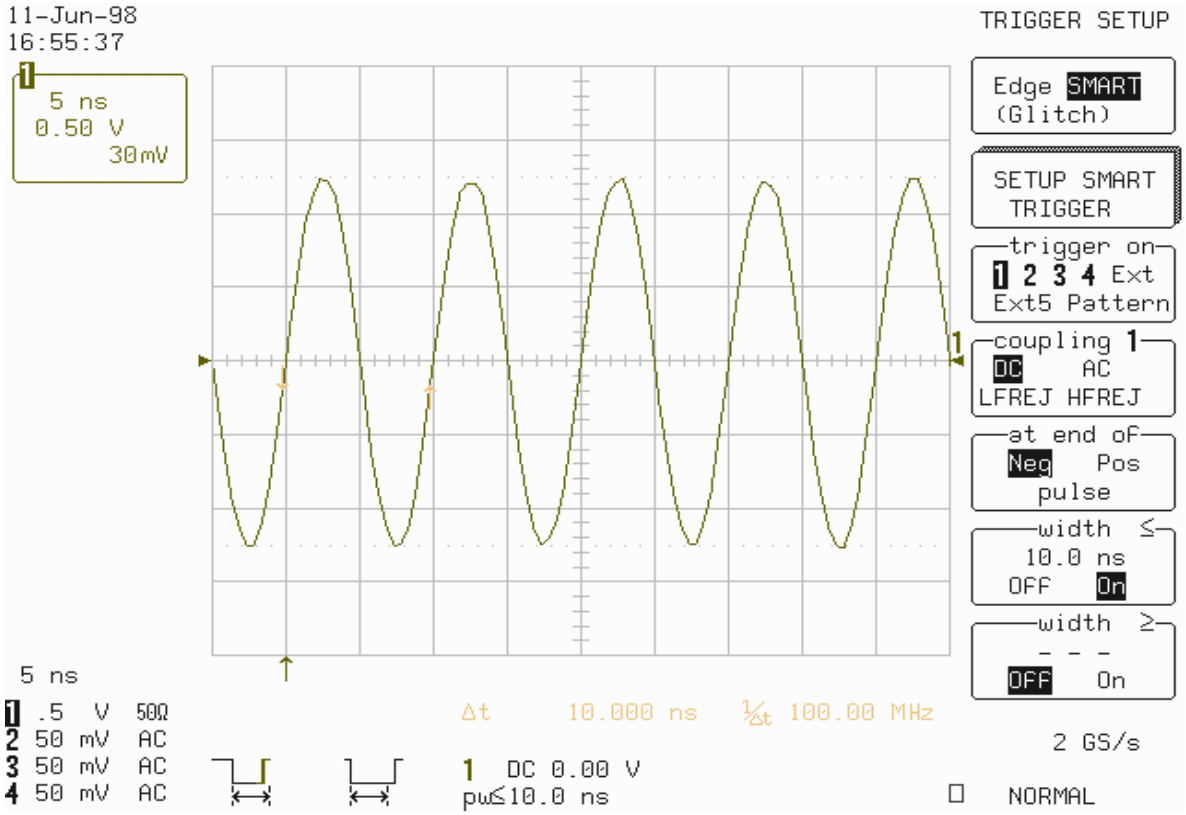
b. Pulse Width > 10 nsec

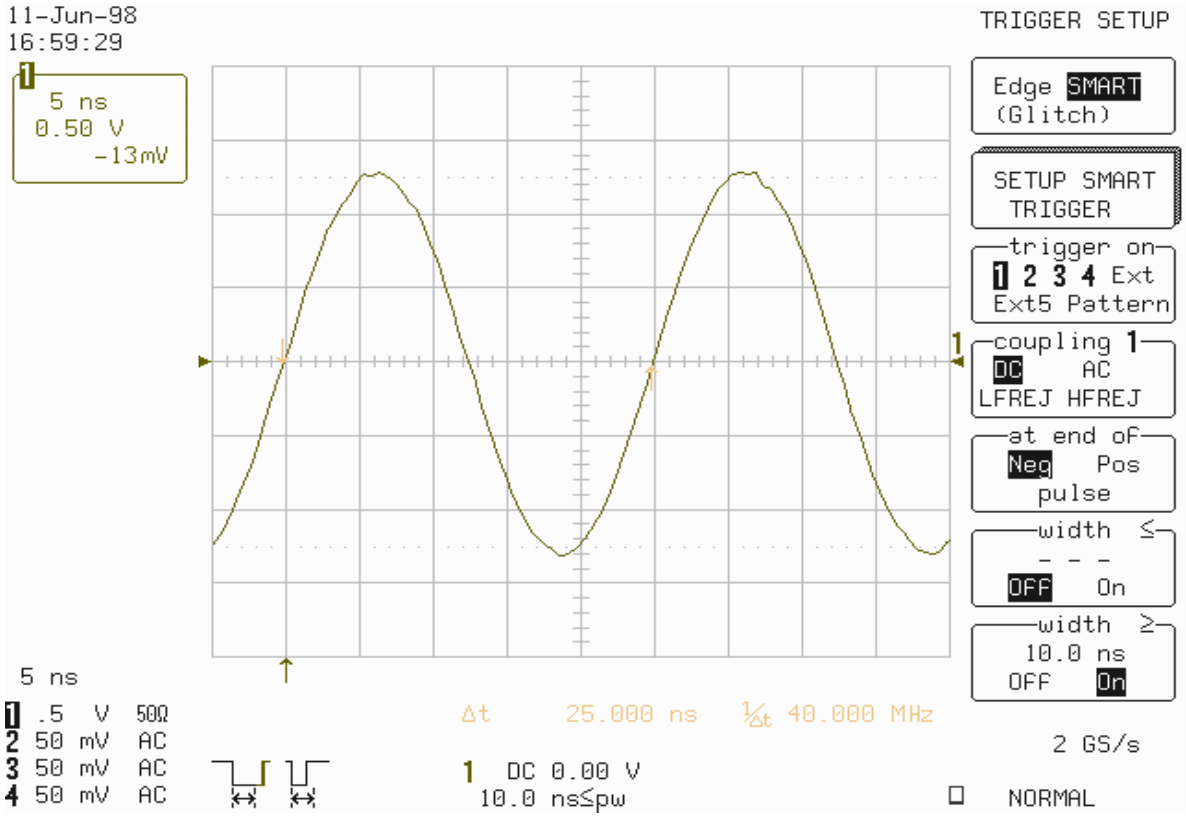
- Set the generator frequency to **40 MHz**.
- Set Width < 10 nsec **Off** and Width > 10 nsec **ON**

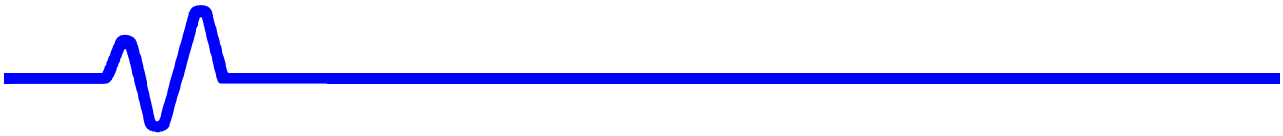
- Check that the scope Triggers. Record the test result in Table 20.

- Set Width < 10 nsec **On** and Width > 10 nsec **Off**

- Check that the scope **doesn't trigger :** slow trigger and no flashes in box. Record the test result in Table 20.


11-Jun-98
16:55:37
TRIGGER SETUP
5 ns
0.50 V
30mV
Edge SMART
(Glitch)
SETUP SMART
TRIGGER
trigger on
1 2 3 4 Ext
Ext5 Pattern
coupling 1
DC AC
LFREJ HFREJ
at end of
Neg Pos
pulse
width ≤
10.0 ns
OFF On
width ≥
- - -
OFF On
5 ns
1 .5 V 50Ω
2 50 mV AC
3 50 mV AC
4 50 mV AC
Δt 10.000 ns 1/Δt 100.00 MHz
2 GS/s
1 DC 0.00 V
pw≤10.0 ns
NORMAL


11-Jun-98
16:59:29
TRIGGER SETUP
5 ns
0.50 V
-13mV
Edge SMART
(Glitch)
SETUP SMART
TRIGGER
trigger on
1 2 3 4 Ext
Ext5 Pattern
coupling 1
DC AC
LFREJ HFREJ
at end of
Neg Pos
pulse
width ≤
- - -
OFF On
width ≥
10.0 ns
OFF On
5 ns
1 .5 V 50Ω
2 50 mV AC
3 50 mV AC
4 50 mV AC
Δt 25.000 ns 1/Δt 40.000 MHz
2 GS/s
1 DC 0.00 V
10.0 ns≤pw
NORMAL



5.11.2 Trigger on Pulse Width 100 nsec

a. Pulse Width < 100 nsec

- Recall **LC564D077.PNL** or configure the DSO as shown in 5.11.1.a and make the following changes :

  Width < 100 nsec : **On**

  Width > 100 nsec **:** **Off**

  Time base : **20 nsec/div.**

- Set the generator frequency to **10 MHz**.
- Check that the scope Triggers. Record the test result in Table 20.
- Set Width < 100 nsec **Off** and Width > 100 nsec **ON**
- Check that the scope **doesn't trigger :** slow trigger and no flashes in box next to normal. Record the test result in Table 20.

b. Pulse Width > 100 nsec

- Set the generator frequency to **4 MHz**.
- Time base : **50 nsec/div.**
- Set Width < 100 nsec **Off** and Width > 100 nsec **ON**
- Check that the scope Triggers. Record the test result in Table 20.
- Set Width < 100 nsec **On** and Width > 100 nsec **Off**
- Check that the scope **doesn't trigger :** slow trigger and no flashes in box. Record the test result in Table 20.

5.12 Time Base Accuracy

5.12.1 Description

An external sine wave generator of **0.1 MHz** with a frequency accuracy better than 1 PPM is used.

Specifications

500 MHz clock : accuracy : ≤ ±**0.001 %** **or** ≤ ±**10 PPM**

5.12.2 500 MHz Clock Verification Procedure

- Recall **LC564D078.PNL** or configure the DSO

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels trace ON		**Channel 1**
Input coupling	:	**DC 50Ω**
Input gain	:	**.1 V/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**1**
Coupling 1	:	**DC**
Slope 1	:	**Pos**
Level 1	:	**100 mV**
Trigger mode	:	**Norm**
Delay	:	**0 %**
Time base	:	**10 µsec/div.**
Channel use	:	**4**
Record up to	:	**50 k**

- Connect the **RF output** of the HP8648B generator through a 5ns 50 Ohm BNC coaxial cable into Channel 1.
- Set the generator frequency to **0.1 MHz**.
- Adjust the generator output amplitude to get **5 divisions peak to peak .**
- Store Channel 1 in Memory 1
- Recall **LC564D079.PNL** or make the following change :
- Set Post-trigger delay to **50.00 msec**
- Recall Memory **1 to A**
- Press : **Cursors/Measure**

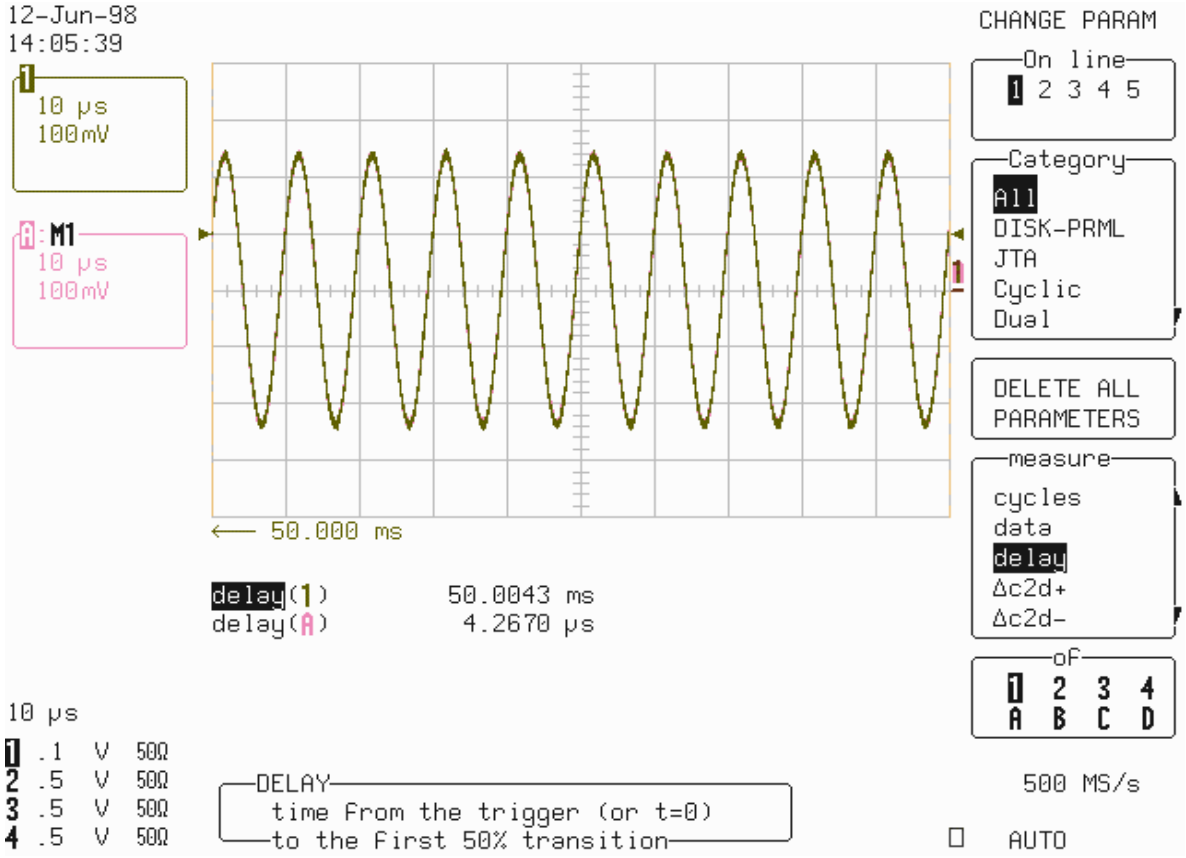
- Measure : **Parameters**
- Mode : **Custom**
- Statistics : **Off**

- Change parameters

- On line 1 : **Delay of 1**
- On line 2 : **Delay of A**

- Check that the displayed Channel 1 trace is **aligned** with the sine wave from memory 1.

- This allows the accuracy of the time base clock to be checked **5000 periods** after the trigger point. A difference of **±0.5 µsec** corresponds to **±10 PPM**.



- Calculate the Difference **{[delay(A) - delay(1)]+ 50 msec}.**

- Record the test result in Table 21, and compare it to the limit in the test record.

5.13 Rise time (10 % - 90 %)

Specifications

DC 50Ω, 50 mV/div., : rise time < 0.50 ns
DC 1MΩ, 100 mV/div., : rise time < 0.90 ns

a. DC 50Ω

- Recall **LC564D080.PNL** or configure the DSO

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels trace ON		**Channel 1**
Input coupling	:	**DC 50Ω** on all 4 Channels
Input gain	:	**0.1 V/div.** on all 4 Channels
Input offset	:	**–250 mV** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**1**
Coupling 1	:	**DC**
Slope 1	:	**Pos**
Level 1	:	**250 mV**
Trigger mode	:	**Norm**
Delay	:	**30 % Pre-Trigger**
Time base	:	**1 nsec/div.**
Channel use	:	**4**
Record up to	:	**50 k**
Turn on trace	:	**A**
Select Math Setup		
For Math	:	**Use at most 1000 points**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg Type	:	**Summed**
Of	:	**Channel 1**
Sweeps	:	**100**
Turn off trace	**:**	**Channel 1**
Cursors/Measure	:	**Parameters**
Mode	:	**Custom**
Statistics	:	**Off**
Change Parameters	:	
On displayed trace	:	**A**
On line 1	:	
Measure	:	**Over + of A**
On line 2	:	
Measure	:	**Rise of A**

- Connect the fast pulse generator 4969A and PB049 power adapter, or equivalent as shown in Figure 5-13.

- Set the 4969A frequency to **1 kHz**

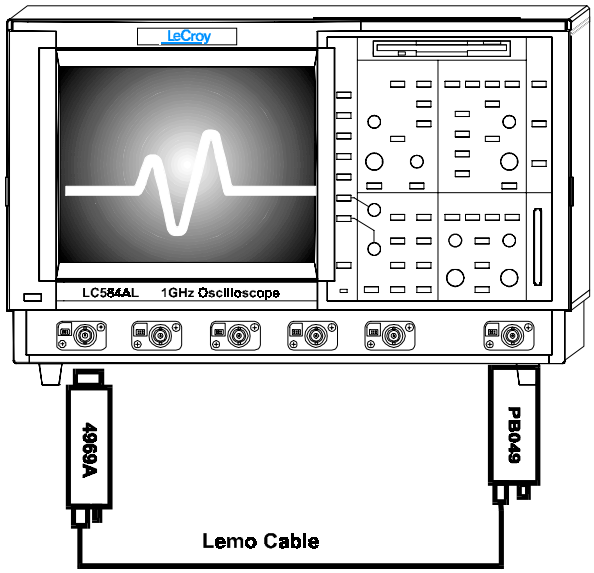


Figure 5-13: 50 Ω Rise time Equipment Setup

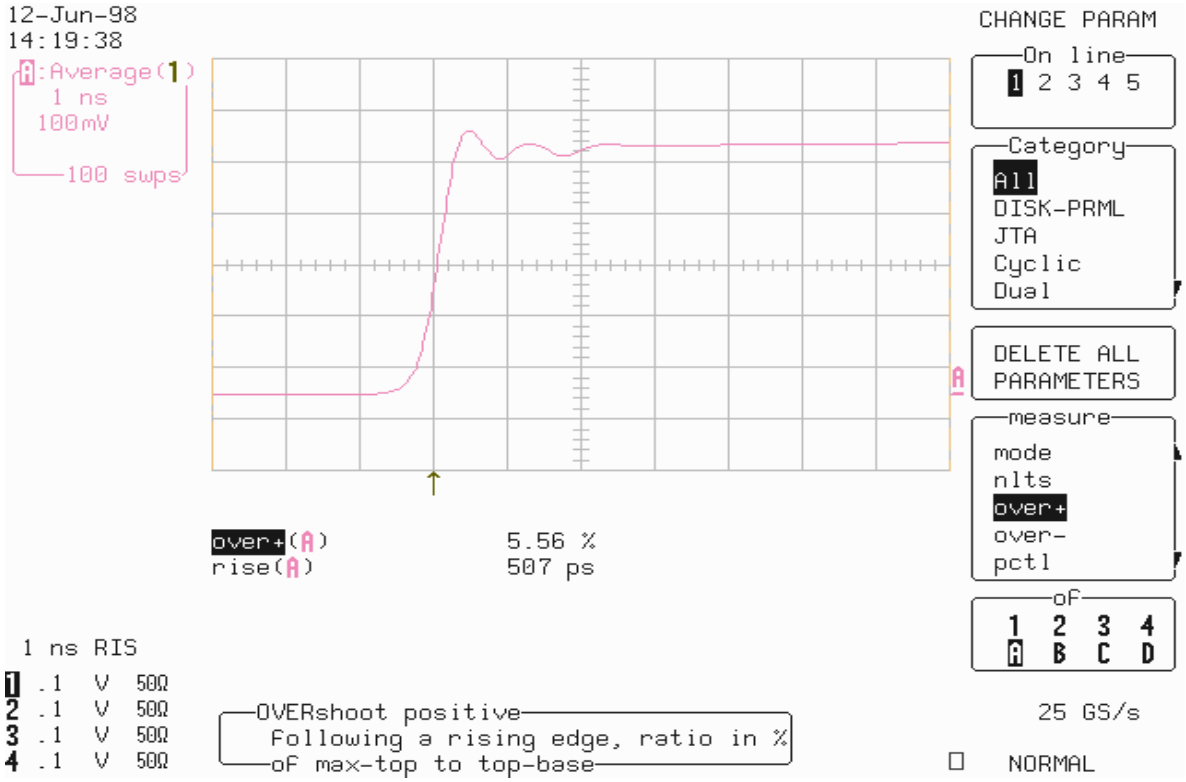
- Press **Clear Sweep**

- After 100 sweeps record **rise(A)** measurements in Table 22**.**

- Repeat the DC 50Ω Rise time test for the other channels, substituting channel controls and input connector.

- Recall **LC564D081.PNL** for Channel 2**, LC564D082.PNL** for Channel3 **LC564D083.PNL** for Channel 4, or configure the DSO as shown in 5.13.a. and make the necessary changes.

- Record the test results in Table 22, and compare the results to the limits.



b. DC 1MΩ

- Recall **LC564D084.PNL** or configure the DSO as shown in 5.13.a. and make the following change :

  Set Input Coupling : **DC 1MΩ** on all 4 Channels
  Input gain : **50 mV/div.** on all 4 Channels
  Input offset : **–150 mV** on all 4 Channels
  Trigger Level : **75 mV**
  Time base : **1 nsec/div.**

- Terminate the output of the 4969A Pulser with the 4962-10 adapter (50Ω to 1MΩ) as shown in Figure 5-14.

- Press **Clear Sweep**. After **100 sweeps** record **rise(A)** in Table22.

- Repeat the DC 1MΩ Overshoot and Rise time test for the other channels, substituting channel controls and input connector.

- Recall **LC564D085.PNL** for Channel 2**, LC564D086.PNL** for Channel3 **LC564D087.PNL** for Channel 4, or configure the DSO as shown in 5.13.a. and make the necessary changes.

- Record the test results in Table 22, and compare the results to the limits.

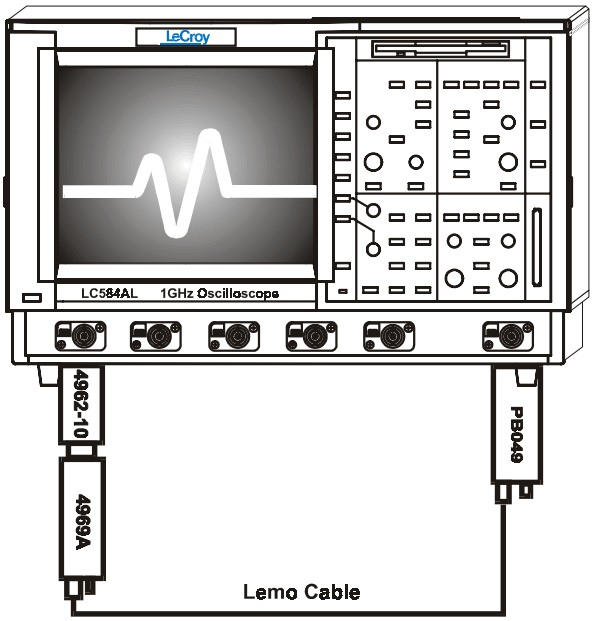
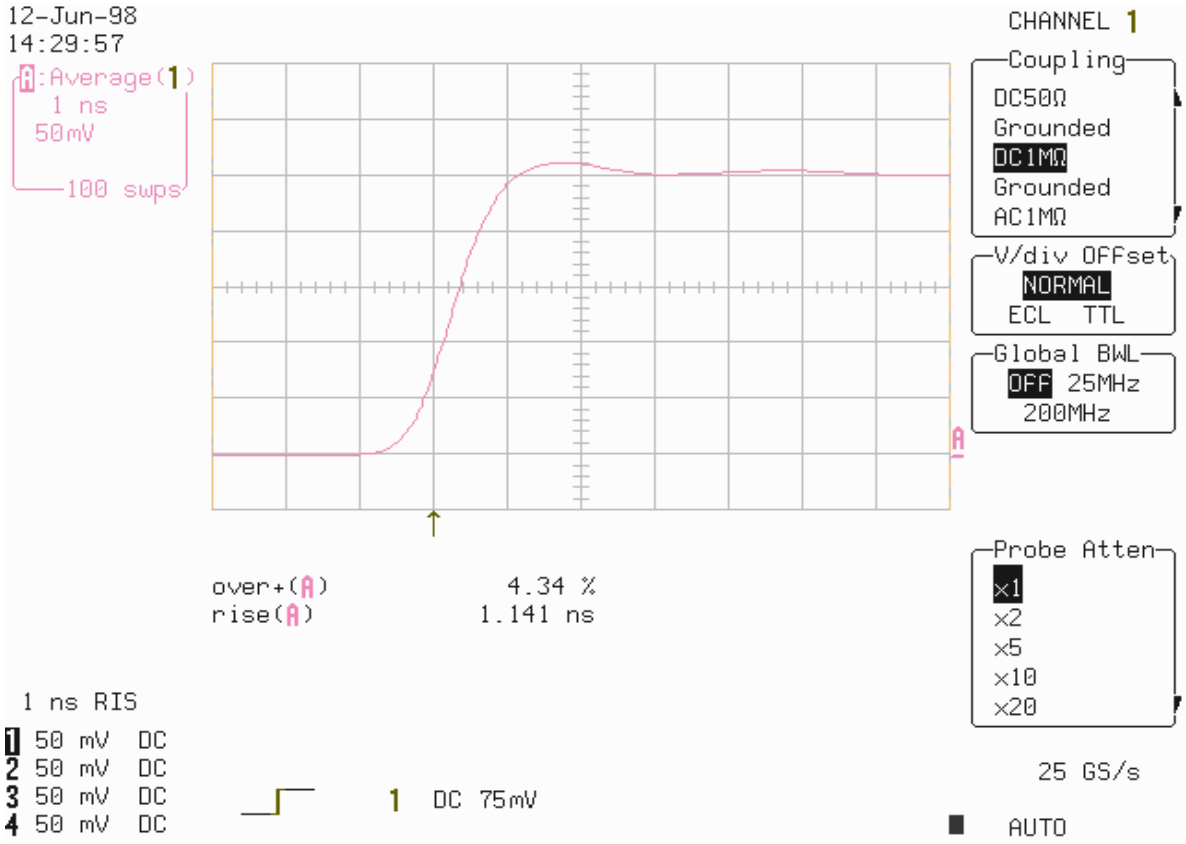


Figure 5-14 : 1MΩ Rise time Equipment Setup



LeCroy Digital Storage Oscilloscope

Performance Certificate

LC564DL Manual Performance Test Procedure Version B – Sept. 2002

Model_____ Serial Number_____ Customer_____

Software Version_____

Inspection Date_____ Next Due_____

Temperature_____ Humidity_____%

Tested By_____ Report Number_____

Place of Inspection_____

Condition found_____ Condition Left_____

Approved By_____

Test Equipment Used

Instrument	Model	S/N	Cal Due Date
Signal Generator Radio Frequency	_____	_____	_____
Signal Generator Audio Frequency	_____	_____	_____
Voltage Generator DC Power Supply	_____	_____	_____
Step Generator Fast Pulser	_____	_____	_____
Digital Multimeter Voltmeter, Ohmmeter	_____	_____	_____

Traceable to_____

Table 1: LC564DL Test Report

Coupling	Volts/div.	Measured Channel 1 Impedance Ω, MΩ	Measured Channel 2 Impedance Ω, MΩ	Measured Channel 3 Impedance Ω, MΩ	Measured Channel 4 Impedance Ω, MΩ	Measured External Impedance Ω, MΩ	Measured External/5 Impedance Ω, MΩ	Lower Limit Ω, MΩ	Upper Limit Ω, MΩ
DC 1MΩ	50 mV/div					N/A	N/A	0.99 MΩ	1.01 MΩ
DC 1MΩ	50 mV/div	N/A	N/A	N/A	N/A			0.98 MΩ	1.02 MΩ
DC 1MΩ	200 mV/div					N/A	N/A	0.99 MΩ	1.01 MΩ
AC 1MΩ	50 mV/div					N/A	N/A	1.006 MΩ	1.047 MΩ
AC 1MΩ	200 mV/div					N/A	N/A	0.98 MΩ	1.02 MΩ
DC 50Ω	50 mV/div					N/A	N/A	49.375 Ω	50.625 Ω
DC 50Ω	200 mV/div					N/A	N/A	49.375 Ω	50.625 Ω
DC 50Ω	50 mV/div	N/A	N/A	N/A	N/A			48.5 Ω	51.5 Ω
Grounded	50 mV/div					N/A	N/A	0.98 MΩ	1.02 MΩ

Table 2: Impedance Test Record

Coupling	Volts/div.	Measured Channel 1 Leakage mV	Measured Channel 2 Leakage mV	Measured Channel 3 Leakage mV	Measured Channel 4 Leakage mV	Measured External Leakage mV	Lower Limit mV	Upper Limit mV
DC 1MΩ	50 mV/div					N/A	–1	+1
DC 1MΩ	200 mV/div					N/A	–1	+1
DC 50Ω	50 mV/div					N/A	–1	+1
DC 50Ω	200 mV/div					N/A	–1	+1
DC 50Ω	50 mV/div	N/A	N/A	N/A	N/A		–1	+1
DC 1MΩ	50 mV/div	N/A	N/A	N/A	N/A		–2	+2

Table 3: Leakage Voltage Test Record

Coupling	Time/Div.	Measured Pkpk Channel 1 mV	Measured Pkpk Channel 2 mV	Measured Pkpk Channel 3 mV	Measured Pkpk Channel 4 mV	Limits mV
DC 1MΩ	20 ms					7.2
DC 1MΩ	1 ms					7.2
AC 1MΩ	2 µs					7.2
DC 50Ω	2 µs					7.2
DC 50Ω	20 µs					7.2
DC 50Ω : 2 Channel Mode	1 µs	disabled			disabled	7.2

Table 4: Peak to Peak Noise Test Record

Coupling	Time/Div.	Measured sdev Channel 1 mV	Measured sdev Channel 2 mV	Measured sdev Channel 3 mV	Measured sdev Channel 4 mV	Limits mV
DC 1MΩ	20 ms					0.72
DC 1MΩ	1 ms					0.72
AC 1MΩ	2 µs					0.72
DC 50Ω	2 µs					0.72
DC 50Ω	20 µs					0.72
DC 50Ω : 2 Channel Mode	1 µs	disabled			disabled	0.72

Table 5: RMS Noise Test Record

Coupling	Volts/div.	Measured Channel 1 Mean (A) mV	Measured Channel 2 Mean (B) mV	Measured Channel 3 Mean (C) mV	Measured Channel 4 Mean (D) mV	Lower Limit mV	Upper Limit mV
DC 1MΩ	2 mV					–0.8	+0.8
DC 1MΩ	5 mV					–2	+2
DC 1MΩ	10 mV					–1.6	+1.6
DC 1MΩ	20 mV					–3.2	+3.2
DC 1MΩ	50 mV					–8	+8
DC 1MΩ	.1 V					–16	+16
DC 1MΩ	1 V					–160	+160

Table 6: DC 1MΩ Ground Line Test Record

Coupling	Volts/div.	Measured Channel 1 Mean (A) mV	Measured Channel 2 Mean (B) mV	Measured Channel 3 Mean (C) mV	Measured Channel 4 Mean (D) mV	Lower Limit mV	Upper Limit mV
DC 50Ω	2 mV					–0.8	+0.8
DC 50Ω	5 mV					–2	+2
DC 50Ω	10 mV					–1.6	+1.6
DC 50Ω	20 mV					–3.2	+3.2
DC 50Ω	50 mV					–8	+8
DC 50Ω	.1 V					–16	+16
DC 50Ω	1 V					–160	+160
DC 50Ω : 2 Channel Mode	.2 V	disabled			disabled	–48	+48

Table 7: DC 50Ω Ground Line Test Record

Volts /div.	Attenuator	P S Output	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
			DMM 1	Mean (A)	Δ 1 Mean– DMM	DMM 2	Mean (B)	Δ 2 Mean– DMM	DMM 3	Mean (C)	Δ 3 Mean– DMM	DMM 4	Mean (D)	Δ 4 Mean– DMM	mV
2 mV	X 100	+0.6 V													±0.8
5 mV	X 100	+1.5 V													±1.2
10 mV	X 100	+3.0 V													±1.6
20 mV	X 100	+6.0 V													±3.2
50 mV	X 10	+1.5V													±8
.1 V	X 10	+3.0 V													±16
1 V	X 1	+3.0 V													±160

Table 8: DC 50Ω, Positive DC Accuracy Test Record

Volts /div.	Attenuator	P S Output	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
			DMM 1	Mean (A)	Δ 1 Mean– DMM	DMM 2	Mean (B)	Δ 2 Mean– DMM	DMM 3	Mean (C)	Δ 3 Mean– DMM	DMM 4	Mean (D)	Δ 4 Mean– DMM	mV
5 mV	X 100	+1.5 V													±1.2
.1 V	X 10	+3.0 V													±16
2V	X 1	+6.0 V													±320

Table 9: DC 1MΩ, Positive DC Accuracy Test Record

Volts /div.	Attenuator	P S Output	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
			DMM 1	Mean (A)	Δ 1 Mean– DMM	DMM 2	Mean (B)	Δ 2 Mean– DMM	DMM 3	Mean (C)	Δ 3 Mean– DMM	DMM 4	Mean (D)	Δ 4 Mean– DMM	mV
2 mV	X 100	– 0.6 V													±0.8
5 mV	X 100	–1.5 V													±1.2
10 mV	X 100	–3.0 V													±1.6
20 mV	X 100	–6.0 V													±3.2
50 mV	X 10	–1.5V													±8
.1 V	X 10	–3.0 V													±16
1 V	X 1	–3.0 V													±160

Table 10: DC 50Ω, Negative DC Accuracy Test Record

Volts /div.	Attenuator	P S Output	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
			DMM 1	Mean (A)	Δ 1 Mean– DMM	DMM 2	Mean (B)	Δ 2 Mean– DMM	DMM 3	Mean (C)	Δ 3 Mean– DMM	DMM 4	Mean (D)	Δ 4 Mean– DMM	mV
5 mV	X 100	–1.5 V													±1.2
.1 V	X 10	–3.0 V													±16
2 V	X 1	–6.0 V													±320

Table 11: DC 1MΩ, Negative DC Accuracy Test Record

Volt /div.	Coupling DC	DSO offset	P S output	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
				DMM 1	Mean (A)	Δ 1 Mean– DMM	DMM 2	Mean (B)	Δ 2 Mean– DMM	DMM 3	Mean (C)	Δ 3 Mean– DMM	DMM 4	Mean (D)	Δ 4 Mean– DMM	mV
2mV	50 Ω	+0.4 V	–0.4 V													±4.8
5mV	50 Ω	+1 V	–1 V													±11.2
5mV	1 MΩ	+1 V	–1 V													±11.2

Table 12: Positive Offset Test Record

Volt /div.	Coupling DC	DSO offset	P S output	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
				DMM 1	Mean (A)	Δ 1 Mean–DMM	DMM 2	Mean (B)	Δ 2 Mean–DMM	DMM 3	Mean (C)	Δ 3 Mean–DMM	DMM 4	Mean (D)	Δ 4 Mean–DMM	mV
2mV	50 Ω	–0.4 V	+0.4 V													±4.8
5mV	50 Ω	–1 V	+1 V													±11.2
5mV	1 MΩ	–1 V	+1 V													±11.2

Table 13: Negative Offset Test Record

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	mW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.200			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.200										0.9	1.1
30.1	0.200										0.9	1.1
300.1	0.200										0.87	1.13
700.1	0.200										0.81	1.19
1000.1	0.200										0.70	N/A

Table 14: DC 50Ω, 50 mV/div. Bandwidth Test Record

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	mW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.800			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.800										0.9	1.1
30.1	0.800										0.9	1.1
300.1	0.800										0.87	1.13
700.1	0.800										0.81	1.19
1000.1	0.800										0.70	N/A

Table 15: DC 50Ω, 100 mV/div. Bandwidth Test Record

Global BWL	Amplitude at 300 kHz	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	Sdev mV	Sdev(1) mV	Freq(1) MHz	Sdev(2) mV	Freq(2) MHz	Sdev(3) mV	Freq(3) MHz	Sdev(4) mV	Freq(4) MHz	MHz	MHz
25	200	140		140		140		140		10	37
200	200	140		140		140		140		110	290

Table 16: DC 50Ω, Bandwidth Limiter Test Record

Frequency	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit
MHz	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3	
0.300	200	N/A	200	N/A	200	N/A	200	N/A	N/A
500.1									0.7

Table 17: DC 1MΩ, 100 mV/div. Bandwidth Test Record

Trigger Level	Trigger Slope	Channel 1	Channel 2	Channel 3	Channel 4	Lower Limit	Upper Limit
mV		Measured DC Trigger Level (1) mV	Measured DC Trigger Level (2) mV	Measured DC Trigger Level (3) mV	Measured DC Trigger Level (4) mV	mV	mV
0	Pos					–30	+30
0	Neg					–30	+ 30
+300	Pos					+250	+350
+300	Neg					+250	+350
–300	Pos					–250	–350
–300	Neg					–250	–350

Table 18: Channel DC Trigger Test Record

Trigger Slope	External Trigger Level	External DC	External Limits		External/5 Trigger Level	External/5 DC	External/5 Limits	
		Measured DC Trigger Level (Ext)	Lower	Upper		Measured DC Trigger Level (Ext5)	Lower	Upper
	mV	mV	mV	mV	V	V	V	V
Pos	0		–50	+50	0		–0.25	+0.25
Neg	0		–50	+50	0		–0.25	+0.25
Pos	+300		+245	+355	+3		+1.7	+4.3
Neg	+300		+245	+355	+3		+1.7	+4.3
Pos	–300		–245	–355	–3		–1.7	–4.3
Neg	–300		–245	–355	–3		–1.7	–4.3

Table 19: External & Ext/5 DC and HFREJ Trigger Test Record

Smart Trigger Pulse Width ns	Generator Frequency MHz	Width <	Width >	Triggered	Pass
< 10	100	On	Off	Yes	
< 10	100	Off	On	No	
> 10	40	Off	On	Yes	
> 10	40	On	Off	No	
< 100	10	On	Off	Yes	
< 100	10	Off	On	No	
> 100	4	Off	On	Yes	
> 100	4	On	Off	No	

Table 20: Smart Trigger Test Record

Generator Frequency MHz	Post Trigger Delay msec	Delay (A) ns	Delay (1) msec	Difference delay(A) –delay(1)+5msec	Lower Limit µsec	Upper Limit µsec
1.00000	5.00000				-0.5	+0.5

Table 21: Time Base Test Record

Coupling	Measured Channel 1 Rise(A) ns	Measured Channel 2 Rise(B) ns	Measured Channel 3 Rise(C) ns	Measured Channel 4 Rise(D) ns	Rise time Limit ns
DC 50Ω					0.50
DC 1MΩ					0.90

Table 22: Rise time Test Record

6. Maintenance

6.1 Introduction

This section contains information necessary to disassemble, assemble, maintain, calibrate and troubleshoot the LeCroy LC564DL digital storage oscilloscopes.

6.1.1 Safety Precautions

The symbol used in this manual indicates dangers that could result in personal injury.

The symbol used in this manual identify conditions or practices that could damage the instrument.

The following servicing instructions are for use by qualified personnel only. Do not perform any servicing other than contained in service instructions. Refer to procedures prior to performing any service.

Exercise extreme safety when testing high energy power circuits. Always turn the power OFF, disconnect the power cord, discharge the cathode ray tube and all capacitors before disassembling the instrument.

6.1.2 Antistatic Precautions

Any static charge that builds on your person or clothing may be sufficient to destroy CMOS components, integrated circuits, Gate array's.....etc.

In order to avoid possible damage, the usual precautions against static electricity are required.

- Handle the boards in antistatic boxes or containers with foam specially designed to prevent static build-up.
- Ground yourself with a suitable wrist strap.
- Disassemble the instrument at a properly grounded work station equipped with antistatic mat.
- When handling the boards, do not touch the pins.
- Stock the boards in antistatic bags.

6.2 Disassembly and Assembly Procedure

The disassembly and assembly procedures detailed below refer to the views of figures shown in section 8.

6.2.1 Disassembly Procedure

Please study the figures in section 8 before attempting disassembly. Before removing any parts from the LeCroy LC564DL, be sure to read carefully the instructions referring to those parts, noting any precautions needed to avoid problems.

Extreme caution should be taken in protecting the LCD face from damage (e.g. scratch marks, fingerprints, dust etc.) when handling, in particular when inserting or removing from the instrument.

a. Removal of the Front Bezel

The front bezel disassembly procedure refers to the view of figure 8-1.

The display is very easily damaged by fingerprints and dust once the front bezel is removed. Extra care must be exercised to protect the LCD face from getting dust or fingerprints. It may be impossible to clean completely if it is touched.

- Before removing front bezel make sure work area is as dust free as possible.
- Cover hands with powder free vinyl gloves.
- Remove three M3X6 screws underneath the plastic bezel.
- Pivot up the plastic bezel and remove it from the front frame by disengaging the hooks on the top of the bezel from the corresponding front frame lugs.
- Place bezel in plastic bag to protect glass from dust and fingerprints.
- Immediately cover LCD face with fresh piece of plastic wrap - secure to frame of unit if nessesary with tape.

b. Removal of the Upper Cover Assembly

The upper cover disassembly procedure refers to the view of figure 8-1.

- Remove the front bezel (6.2.1.a)
- Remove the seven M3X6 screws (three M3X6 on top, two M3X6 on left and two M3X6 on right).
- Remove the two upper feet ruber (see 11 on figure 8-3).
- Remove the two M5 screws that secure the two upper feet to the upper cover and rear panel.
- Carefully slide the upper cover off the unit (disconnect optional Internal printer cables from power supply and processor board).

c. Removal of the Front Frame Assembly with Color LCD Display

The front frame disassembly procedure refers to the view of figure 8-2 and 8-12.

- Remove the front bezel (6.2.1.a)
- Remove the upper cover assembly (6.2.1.b)
- Remove two M3X6 screws that secure the front frame on both side of the lower cover.
- With a long hex screwdriver unlock four M3X6 screws that secure the front frame on the main board upper shield.
- Disconnect the monitor cable from the F9615-21 card connector J1
- Disconnect the floppy cable from the processor board connector J1.
- Disconnect the front panel cable from the processor board connector J2

The front frame assembly with LCD display, front panel and floppy disk drive can with care be removed forward from the unit.

d. Removal of the Processor Board

The processor board disassembly procedure refers to the view of figure 8-1 & 8-18.

- Remove the front bezel (6.2.1.a)
- Remove the upper cover assembly (6.2.1.b)
- Remove the front frame assembly (6.2.1.c)
- Disconnect the processor cable J10 from the F9601-2 card connector J4.
- Disconnect the processor cable J9 from the F9301-4 RS232 & GPIB interface. and optional F9300-8 hard disk interface.

The processor can now be removed vertically from the main board connector J1.

e. Removal of the Power Supply Assembly

The power supply disassembly procedure refers to the view of figure 8-3.

- Remove the front bezel (6.2.1.a)
- Remove the upper cover assembly (6.2.1.b)
- Remove the front frame assembly (6.2.1.c)
- Remove the processor board (6.2.1.d)

If the instrument is equipped with hard disk option, remove the F9300-8 interface from the rear panel, by removing two M3X6 screws that secure it to the rear panel.

- Remove two M3x6 screws that secure the fan shroud to the rear panel.
- Remove one M3x6 screw which secures the fan shroud to the top of the power supply.

- Remove two M3X6 screws that secure the power supply on the main board upper shield.
- Remove two M3X6 screws that secure the power supply on the rear panel.
- Disconnect the power supply cable from the F9601-8 board connector J2
- Disconnect the fan power cable from the power supply connector J6

The power supply can now be removed vertically from the oscilloscope.

f. Removal of the Upper Shield Assembly

The upper shield disassembly procedure refers to the view of figure 8-2, 8-3 & 8-4.

- Remove the front bezel (6.2.1.a)
- Remove the upper cover assembly (6.2.1.b)
- Remove the front frame assembly (6.2.1.c)
- Remove the processor board (6.2.1.d)
- Remove the power supply assembly (6.2.1.e)
- Remove the two M3x5 that secure the fan shroud to the rear panel.
- Remove twelve M3x20 screws that secure the shield to the lower cover.
- Remove six M3X5 screws on both side of the lower cover.
- Remove six M2.5x6 screws that secure the upper shield to the main board front panel.
- Remove three M3X6 screws that secure the upper shield to the rear panel.
- Disconnect the power cable from the F9601-8 board connector J1.

The upper shield can now be removed from the oscilloscope.

g. Removal of the Rear Panel Assembly

The rear panel disassembly procedure refers to the view of figure 8-3 & 8-8.

- Remove the front bezel (6.2.1.a)
- Remove the upper cover assembly (6.2.1.b)
- Remove the front frame assembly (6.2.1.c)
- Remove the processor board (6.2.1.d)
- Remove the power supply (6.2.1.e)
- Remove the upper shield (6.2.1.f)
- Remove the two lower feet rubber (see 5 on figure 8-4)
- Remove two M5 screws that secure the two lower feet to the rear panel and lower cover.

The rear panel assembly can now be removed from the oscilloscope.

h. Removal of the Main Board Assembly

The main board disassembly procedure refers to the view of figure 8-5 & 8-10.

- Remove the front bezel (6.2.1.a)
- Remove the upper cover assembly (6.2.1.b)
- Remove the front frame assembly (6.2.1.c)
- Remove the processor board (6.2.1.d)
- Remove the power supply (6.2.1.e)
- Remove the upper shield (6.2.1.f)
- Remove three M3x6 screws that secure the main board to the lower cover.
- Remove twelve M3X6 screws that secure the main board to the lower cover

The main board can now be removed from the oscilloscope.

6.2.2 Assembly Procedure

Reassemble the unit in the reverse order, check that all screws shown on the drawings in section 8 are used and properly torqued.
Verify that all cables are correctly connected.

Assembly Note :

- **Bezel :** The plastic bezel should be in contact with the CRT all around the screen area. The bezel should not be deformed. When reassembling unit, if glass on inside of bezel must be cleaned use lint free wipes and while again wearing a lab coat and gloves try to polish off any marks, as a last resort use glass cleaner. If any fingerprints are present on LCD display, it may be possible to clean with alcohol and a lint free wipe, however sometimes it is impossible to clean it completely. If dust is present it may be possible to blow it off using particle free compressed air however this may cause more dust to be drawn to the LCD face.

- **LCD Display**: Being careful not to damage the LCD face. Fingerprints may be impossible to clean off.

- **Fan** : Check the fan cable direction. Note the air flow, the fan extracts air from the unit and expels it.

- **Feet** : Check that the lower feet and rear feet are aligned and properly tightened before re-assembly.

- **Filter** : Check that the earth wire is correctly installed and tightened.

- **Floppy** : Adjust the floppy position to obtain the front face tangential to face of the front panel. Check that the door is moving freely and shuts correctly.
  Insert a floppy and eject it to check the mechanism.

- **Front Panel** : Check that knobs rotate freely, are the right size and in the right place.
- **Main Board** :The main card must be parallel and tacked against the bend of the lower cover. Being careful not to bend the board or damage components underneath.
- **Rear Panel** : Check the CD9610 trimming adjustments align with holes in the rear panel.
- **Processor** : Check that the memory card insertion guide is correctly inserted in the front panel.
- **Printer** : If the graphic printer is used, before closing don't forget to plug input cable to the option and the driver cable to the processor card.

6.3 Software Update Procedure

6.3.1 Firmware upgrades are available from the Internet via http://www.lecroy.com or CDROM using the LeCroy software utility Scope Explorer.

The following methods are available for upgrading scope firmware:

1) GPIB **2) RS-232** **3) Floppy disk (No connection)**

Each method is described below.

a) GPIB:

Scope requirements:
- IEEE 488.2 GPIB cable connected to the PC.
- From the utilities menu; select the GPIB/RS232 menu.
- Now select a GPIB address and ignore the rest of the menu.
- Put the scope in stop mode by depressing STOP on the front panel.

PC requirements:
- National Instruments TNT type GPIB card.
- Windows 95, 98, or NT operating system.
- LeCroy Scope Explorer utility.

Connecting to PC
1) Open Scope Explorer, then select Scope-finder from the scope pull-down menu. (see fig. #1)
2) From the Scope-finder window select find.
3) If more than one device appears in the window, select the correct device.
4) Using the scope pull-down menu select upgrade DSO from internet/CD and follow the upgrade wizard. (see fig. #2)
5) After following the instructions, the firmware will be automatically upgraded via the Internet.

6) Cycle the power when prompted.

b) RS232:

Scope requirements:

- 9-pin serial null modem cable connected to the PC.
- From the scope utilities menu; select the GPIB/RS232 menu.
- Select RS232; 8 bits; parity none; stop bits 1; max baud rate 19.2K; and ignore the GPIB address.
- Place scope in stop mode by depressing STOP on the front panel.

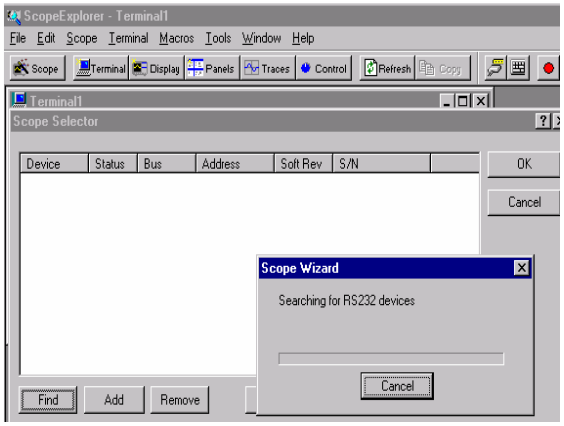


Figure 1: scope find window

PC requirements:

- Windows 95, 98, or NT operating system
- LeCroy Scope Explorer utility.
- Two 1.44 M byte formatted floppy disks

Connecting to PC

1) Open Scope Explorer, then select Scope-finder from the scope pull-down menu (see fig. #1)
2) From the Scope-finder window select find.
3) If more than one device appears in the window, select the correct device.
4) Using the scope pull-down menu select upgrade DSO from internet/CD and follow the upgrade wizard (see fig. #2)
5) The scope cannot be upgraded directly through RS232, but will download the firmware to 1.44 Mbyte floppy disks.
6) After the software is loaded to the floppy disks, put floppy # 1 into the scope drive.
7) Push the utilities button and select special modes from the on screen menu.
8) Now select firmware update, and update from floppy.
9) From the on screen menu choose update flash.
10) Remove floppy # 1 and insert floppy # 2 into scope when prompted on scope display.
11) Cycle the power when prompted.

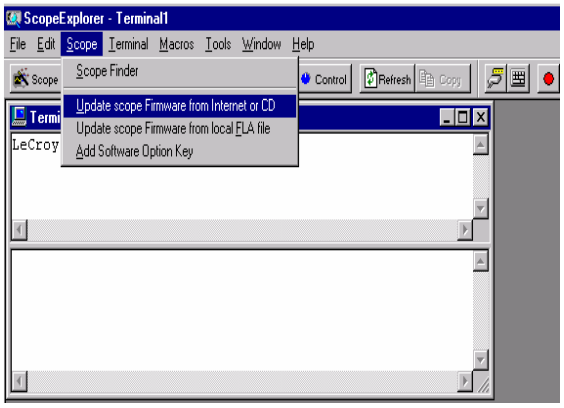


Figure 2: firmware upgrade window

c) No Connection (floppy disk)

Scope requirements:
- Put the scope in stop mode by depressing STOP on the front panel.

PC requirements:
- Windows 95, 98, or NT operating system.
- LeCroy Scope Explorer utility.
- Two 1.44 Mbytes formatted floppy disks.

Without a connection:
1) Open Scope Explorer
2) Using the scope pull-down menu select upgrade DSO from internet/CD and follow the upgrade wizard
3) You must have the scope model number, the firmware version, and the scope serial number.
4) To find the scope information, push the show status button on the scope.
5) In the status box, highlight system by pressing the second on screen menu button and the text screen will contain the necessary information.
6) Because the scope cannot upgrade directly Scope Explorer will download the firmware to 1.44 Mbytes floppy disks.
7) Now follow the same directions as RS232 connection step # 6

6.3.2 Software Options

The following software options are available:

- WP01 Advanced Math Firmware
- WP02 Basic FFT Firmware
- WP03 Parameter Distribution Analysis Firmware
- DDM Disk Drive Measurements
- PRML Partial Response Maximum Likelihood
- ORM Optical Recording Measurement
- DDFA Disk Drive Failure Analysis
- MC01 PCMCIA Memory Card
- JTA Jitter and Timing Analysis
- PMT Power Measurement Tools
- MT01/02 Automatic Mask Tester
- MT03 OC3/OC12 Optical Signal Test Solution
- PMSK Polymask Mask Testing Software
- JPRO JitterPro
- CCTM Clock Certification and Test Module

6.3.2.1 Changing Software Option Key

a. Scope ID, Scope Serial Number

The scope ID and scope s/n: are used to request a Software Option Key

- Enter the scope's Software Options menu (located under the **STATUS**, **SYSTEM** menu).
- Note the **SCOPEID**, i.e: 59258A-31 and **Scope s/n**: LC564DL30104 that are found on that menu.

b. Entering Option Key in the DSO

- Enter the scope's Software Options menu (**STATUS**, **SYSTEM** menu).
- Enter the **ADD OPTION KEY** menu on the DSO
- Enter the new option key using the dymo-editor, i.e: **C4B5-F4A9-4464-E7ED**
- Click on **ENTER THIS OPTION KEY** to add the key
- Reboot the scope and verify that the options added correctly.

6.3.3 Processor Board Exchange Procedure

The serial number of the LC564DL oscilloscope is loaded in the real time clock memory which is battery backed up. If it becomes necessary to replace the processor board, the serial number must be loaded in the memory of the new board by using LeCroy program " LeCalsoft " under GPIB remote control.
To run " LeCalsoft " type SKP.exe, in the main menu type S, and follow the instructions, use five digits to enter the serial number (i.e. 30104).
Then check in the system summary, by using the show status button on the front panel, the scope serial number.

6.4 Equipment and Spare Parts Recommended for Service

6.4.1 Test Equipment Required

See Table 5-1 in section 5.2.

6.4.2 LC564DL Spare Parts

LeCroy P/N	Assembly	Adjustments	Performance Tests
F9601-11-16	Power PC, 2X8MB DRAM	None	None
F9601-2	Internal + External VGA Centronics Interface	None	None
900079	Acquisition Card 4 GS/s	None	See Chapter 5
F9301-4	GPIB Interface RS232 Interface	None	None
F9615-5	Keyboard Assy	None	None
S9615-21	Buffer Board	None	None
F9601-6	Floppy Disk Drive Assy	None	None
F9300-7	Printer Interface	None	None
F9300-8	Hard Disk Interface	None	None
F9601-9	NMB Variofan	None	None
S9601-9	NMB Speed Control	None	None
258104001	TFT Color LCD Module, 10.4 inch	None	None
PS9611	Power Supply	6.5.1	None

The other parts are not on the above list because the probability of failure is very low. See chapter 7, 8 & 9 for mechanical and electrical replaceable parts.

6.5 Calibration Procedures

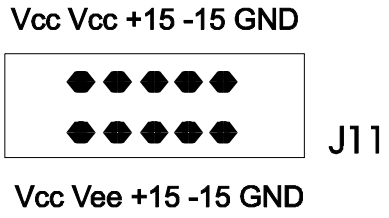
The following section includes the manual adjustments of the power, but does not contain any instructions or descriptions about the acquisition board calibration. The acquisition board adjustments required complex test set-up and calibration Software. For information on the availability of the tester and software, contact your nearest LeCroy service center.

6.5.1 Power Supply Calibration Procedure

- Remove the front bezel (see 6.2.1.a)
- Remove the upper cover assembly (see 6.2.1.b)

- To ensure adequate main board cooling, it is necessary to control the air flow by installing a **temporary closure plate** which fully encloses the air space behind the monitor.

- Turn on the power, set the scope to **Auto Trigger**, and perform the adjustments to get on processor board connector J11:



Vcc : **+ 5.00V** (Min = + 4.9 V, Max = + 5.10 V)
Vee : **- 5.1 V** (Min = - 5.05 V, Max = - 5.15 V)
+15 : **+14.95 V** (Min = +14.90 V, Max = +15.05V)
- 15 : **- 14.95 V** (Min = -14.90 V, Max = -15.05 V)

- The four potentiometers are accessible from the top through holes in the PS9611 power supply chassis.

- Turn the potentiometer clockwise to increase the voltage or counterclockwise to decrease the voltage.

- When the adjustment is done, stop the acquisition by depressing the stop trigger push button, and verify that there is no large difference on the + 5.00 V, typically less than 80 mV.

6.6 Troubleshooting and Flow Charts

6.6.1 Introduction

The troubleshooting information contained in this section is intended for use by qualified personnel having a basic understanding of electronics (analog and digital). In order to simplify servicing and minimise downtime, the following list of possible symptoms, likely causes, and troubleshooting steps have been prepared. The first step in troubleshooting is to check for obvious items like blown fuses. The power supply is the next item to check before proceeding to more detailed troubleshooting, since noise or low power supply voltages can cause a variety of digital and analog problems.

6.6.2 Line Fuses Replacement

The power supply of the oscilloscope is protected against short circuits and overload by means of two T6.3A / 250 V fuses located above the main plugs.

Turn off the power and disconnect the line cord from the instrument Disconnect the instrument from other equipment.

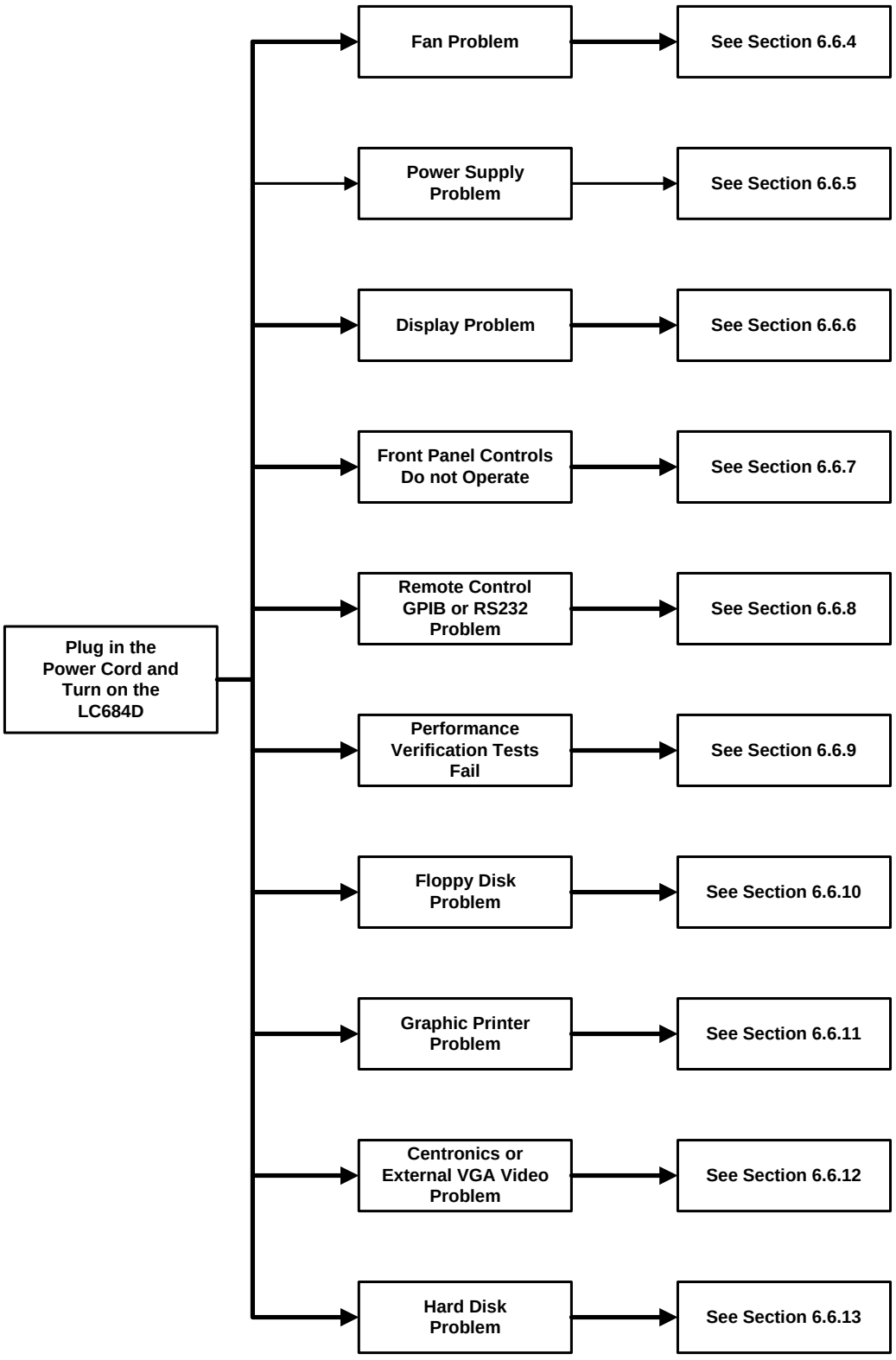
To replace line fuses, proceed as follow:

- Open the fuse box by inserting a small flat screwdriver under the plastic cover and remove the fuse carrier from the holder
- Remove the fuse and replace it with the proper type: T6.3 A / 250 V, LeCroy part number: **433 162 630**

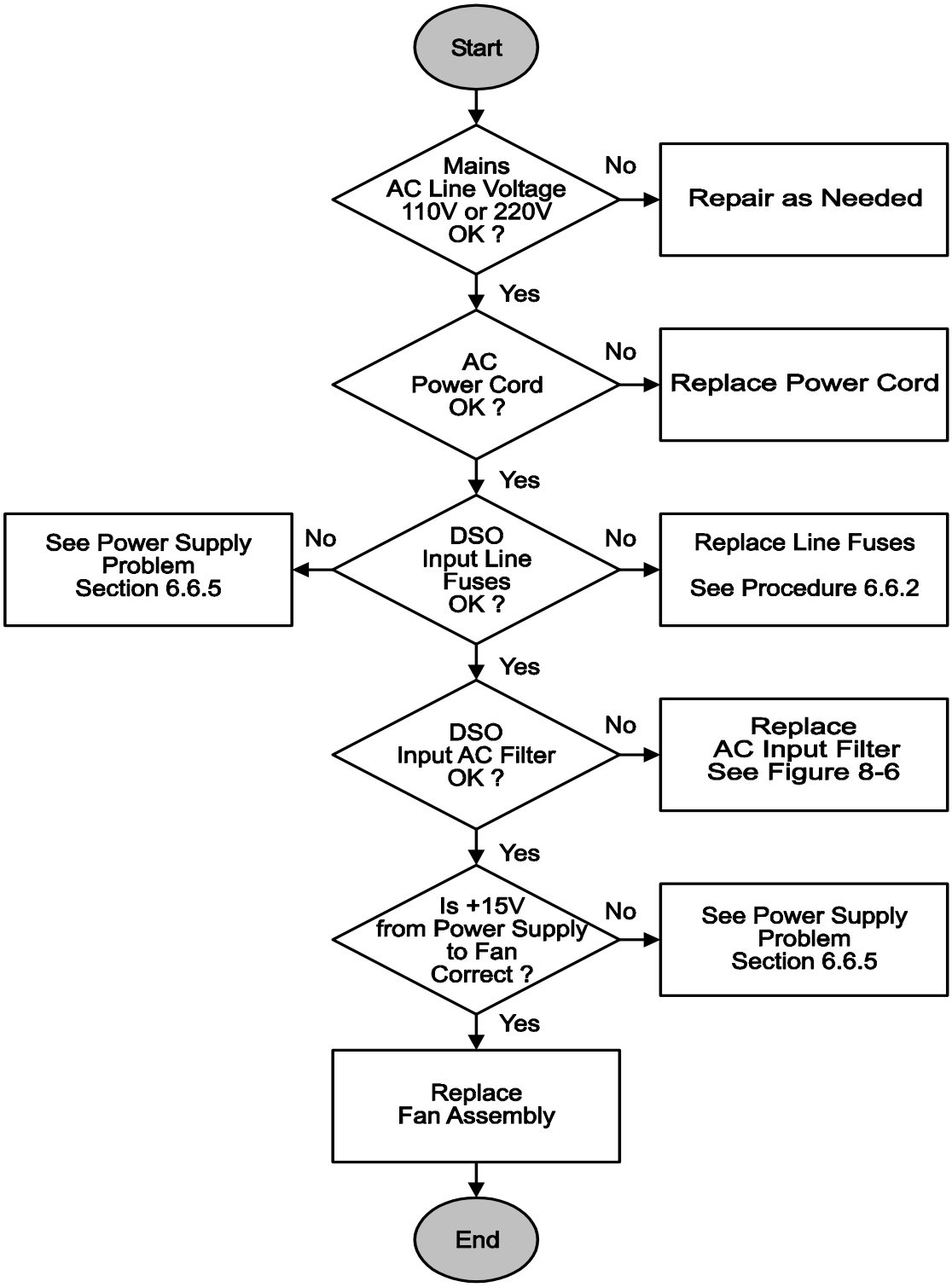
6.6.3 Initial Troubleshooting Chart

Most procedures in this section will allow troubleshooting down to the **BOARD LEVEL.**

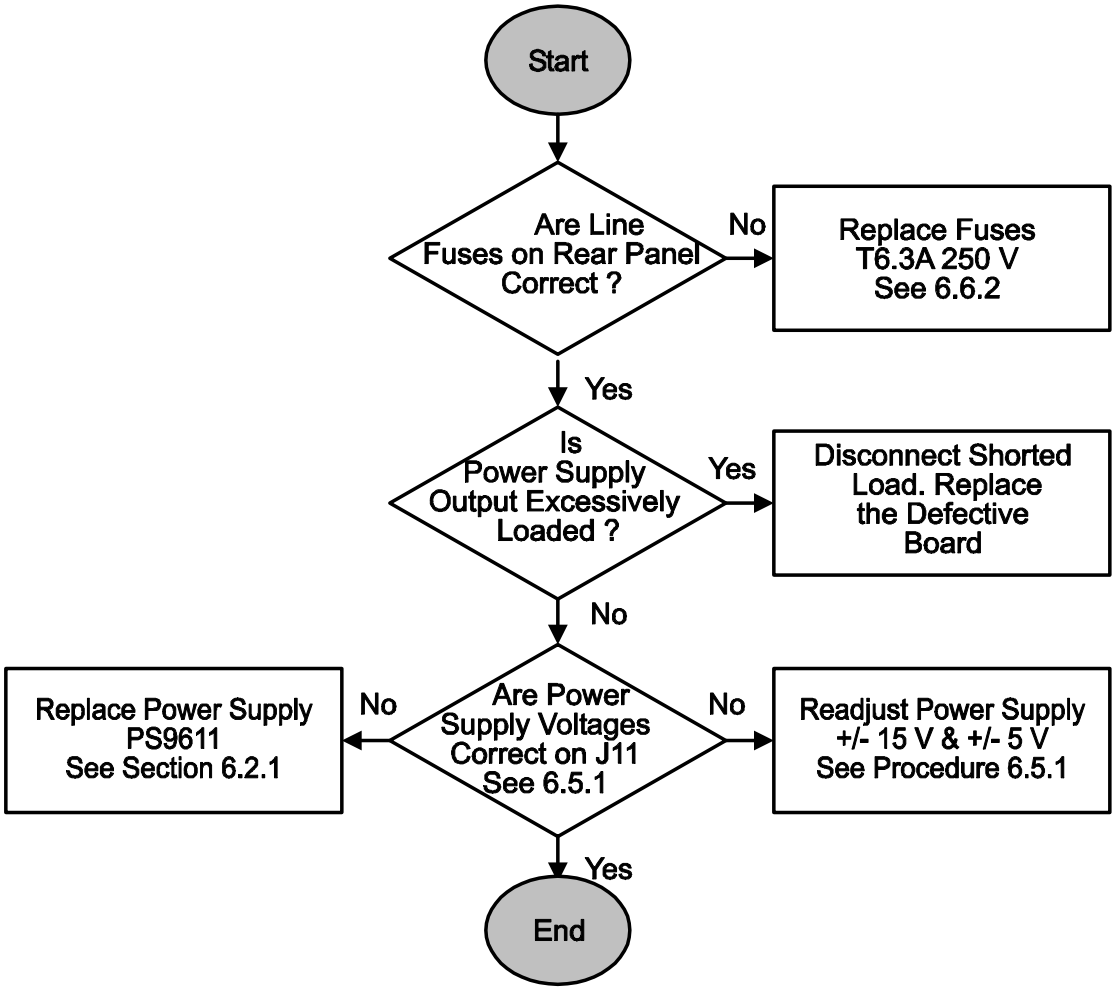
Defective circuit boards will be repaired or exchanged by the regional LeCroy service office or the local representative (see section 2.2).


Plug in the Power Cord and Turn on the LC684D
Fan Problem
See Section 6.6.4
Power Supply Problem
See Section 6.6.5
Display Problem
See Section 6.6.6
Front Panel Controls Do not Operate
See Section 6.6.7
Remote Control GPIB or RS232 Problem
See Section 6.6.8
Performance Verification Tests Fail
See Section 6.6.9
Floppy Disk Problem
See Section 6.6.10
Graphic Printer Problem
See Section 6.6.11
Centronics or External VGA Video Problem
See Section 6.6.12
Hard Disk Problem
See Section 6.6.13

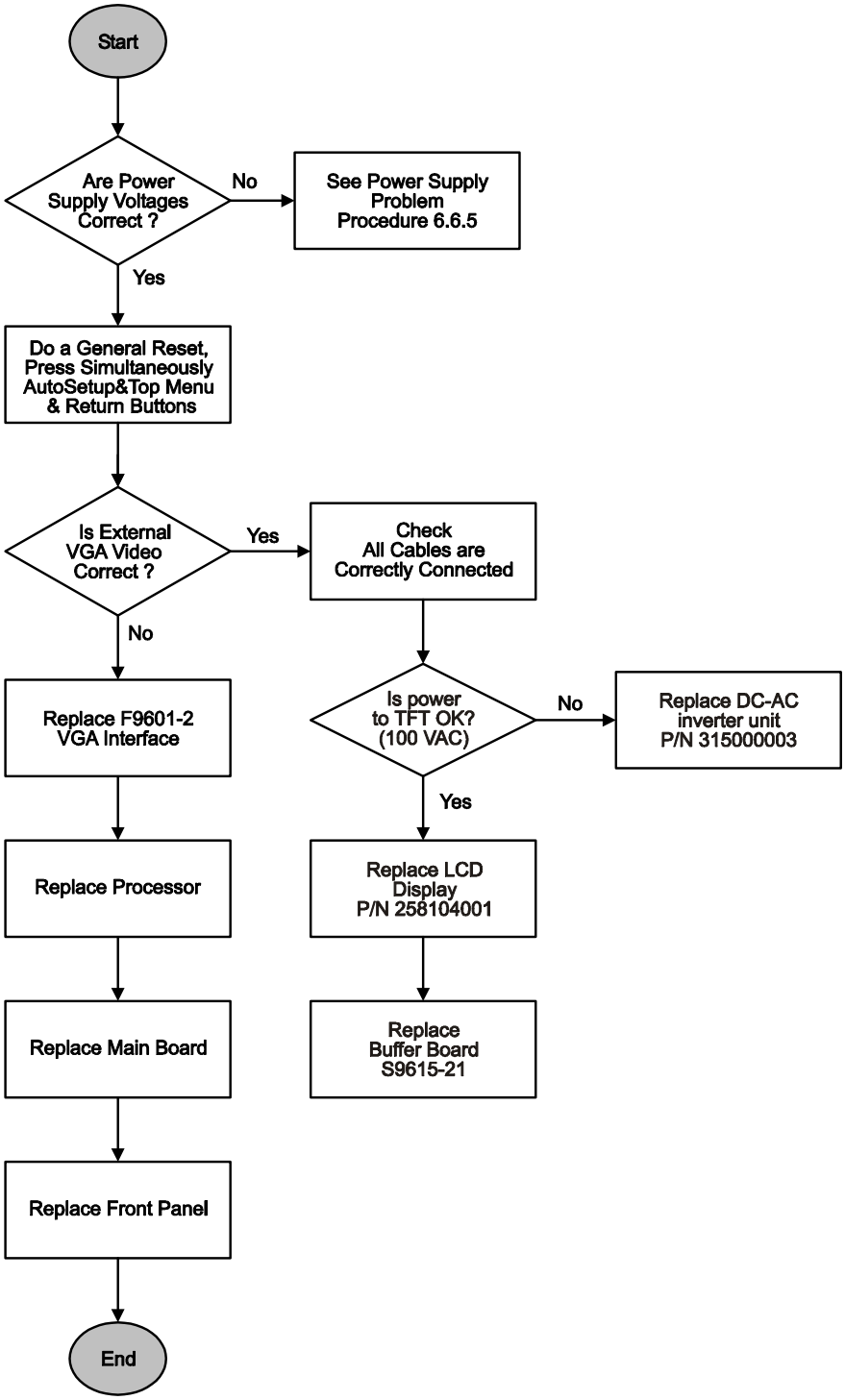
6.6.4 Fan Problem



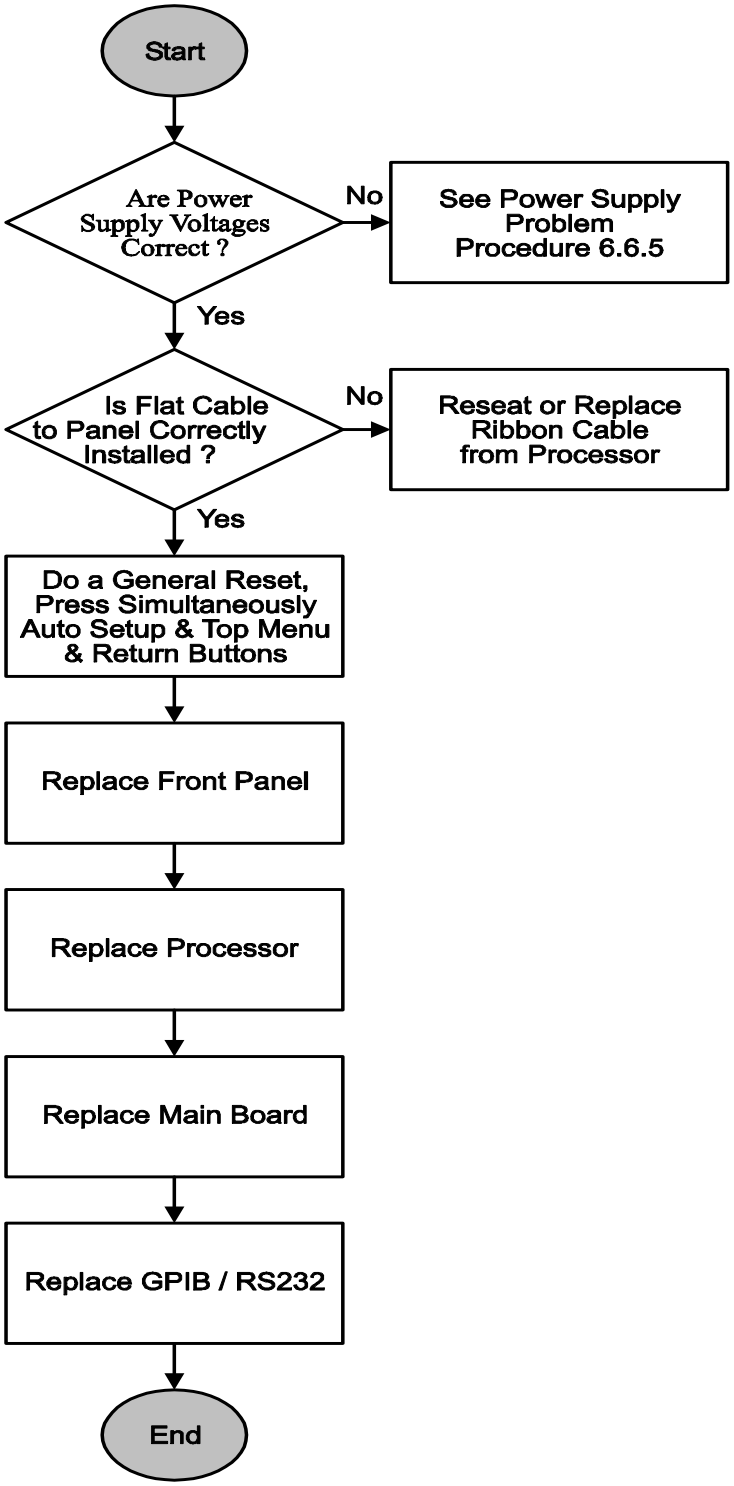
6.6.5 Power Supply Voltages Problem



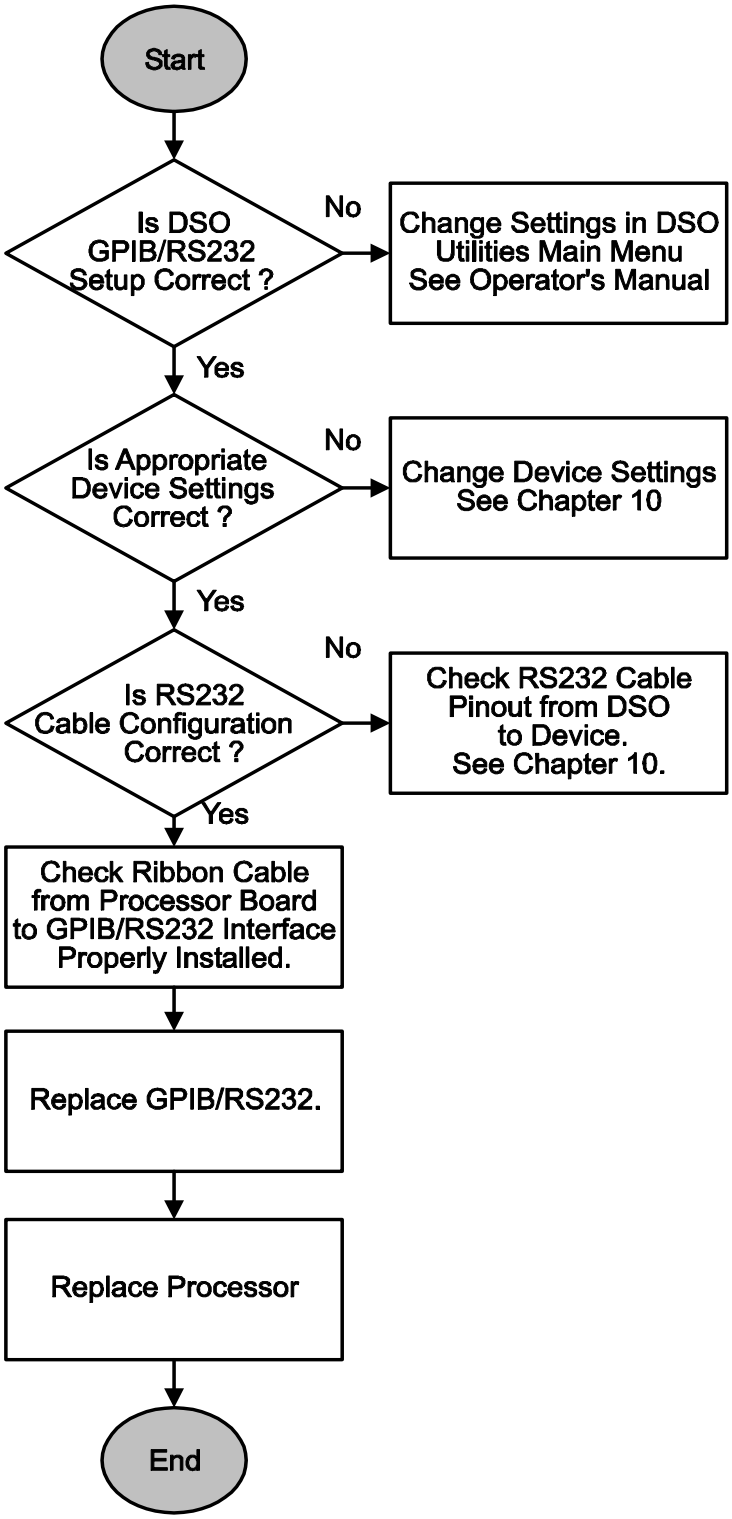
6.6.6 Display Problem



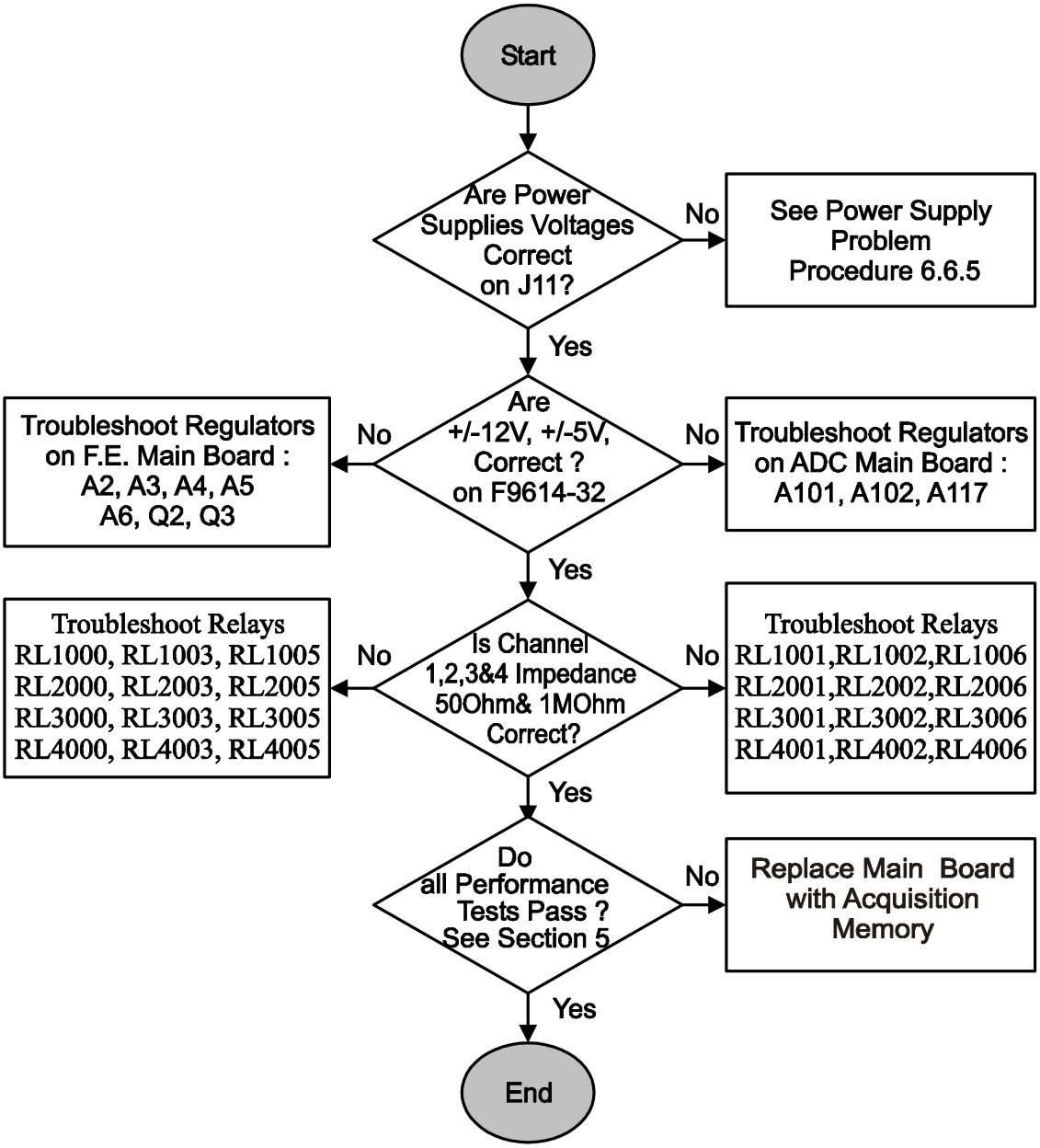
6.6.7 Front Panel Controls Do not Operate



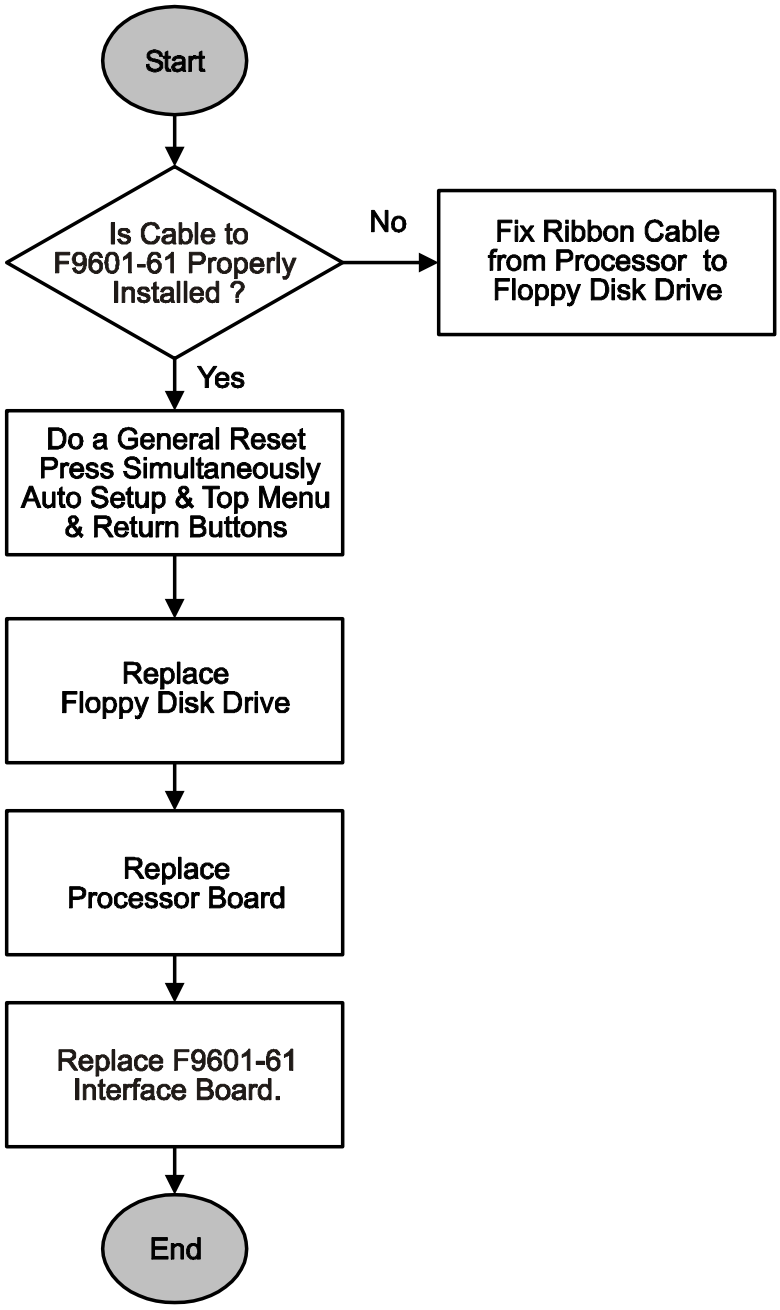
6.6.8 Remote Control GPIB or RS232 Problem



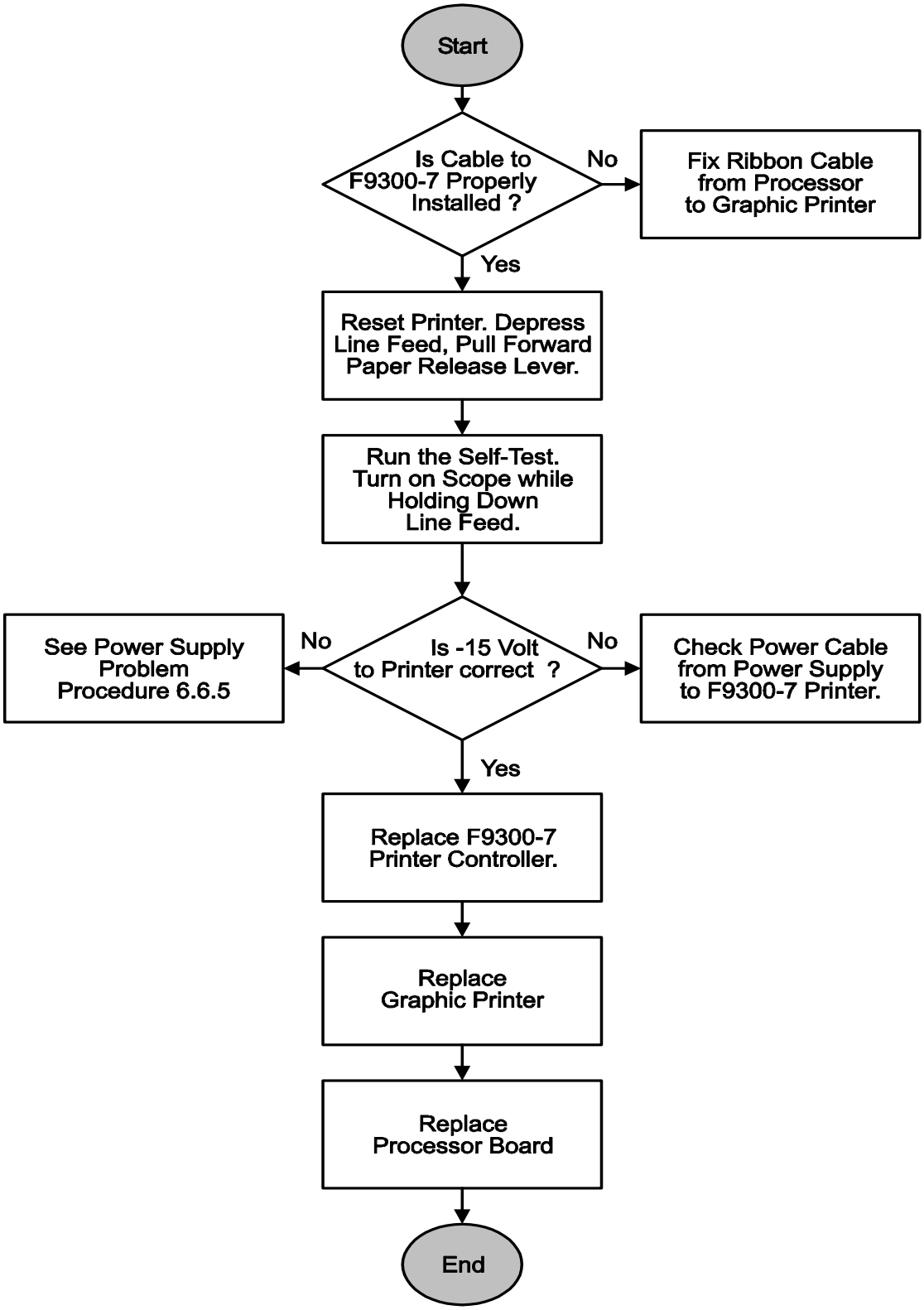
6.6.9 Performance Verification Fails



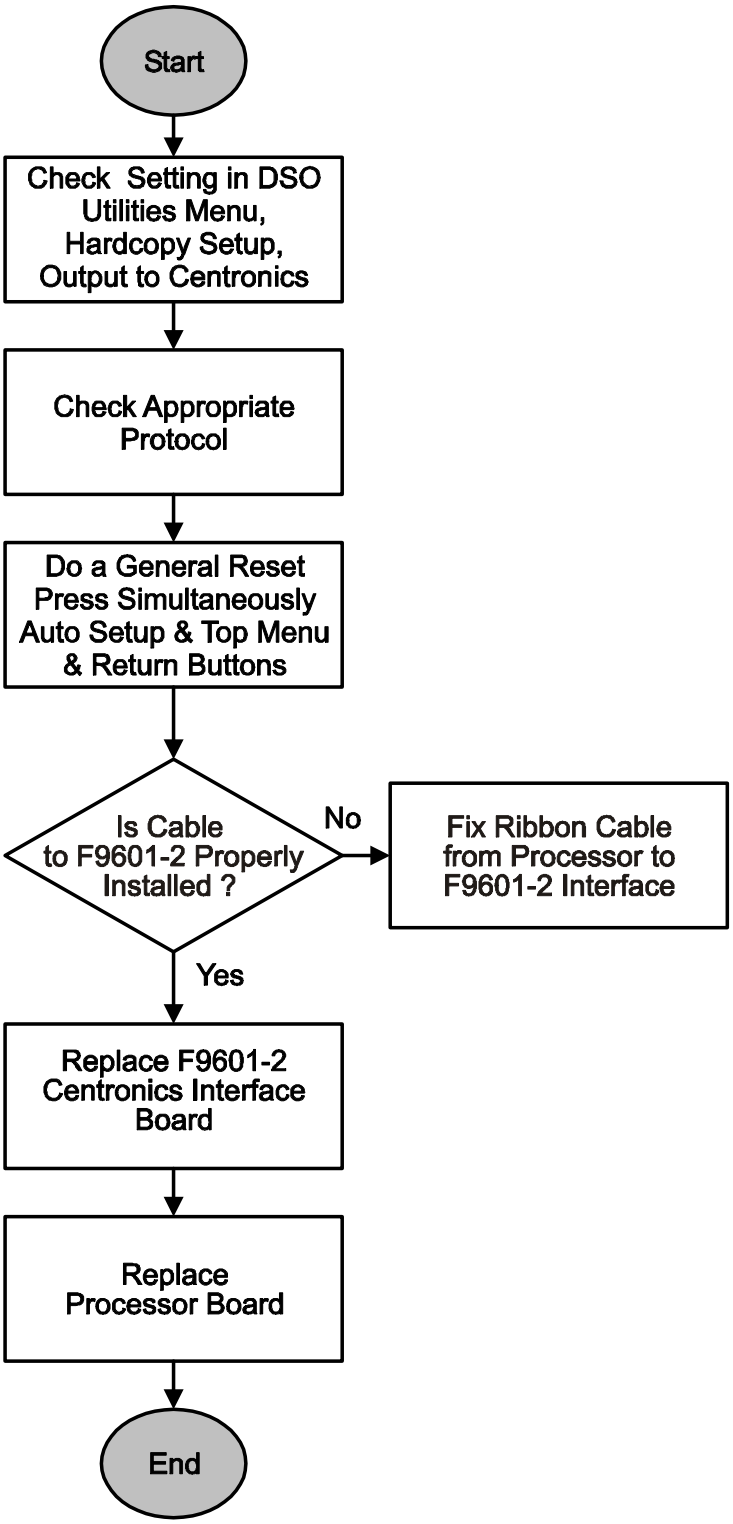
6.6.10 Floppy Disk Drive Problem



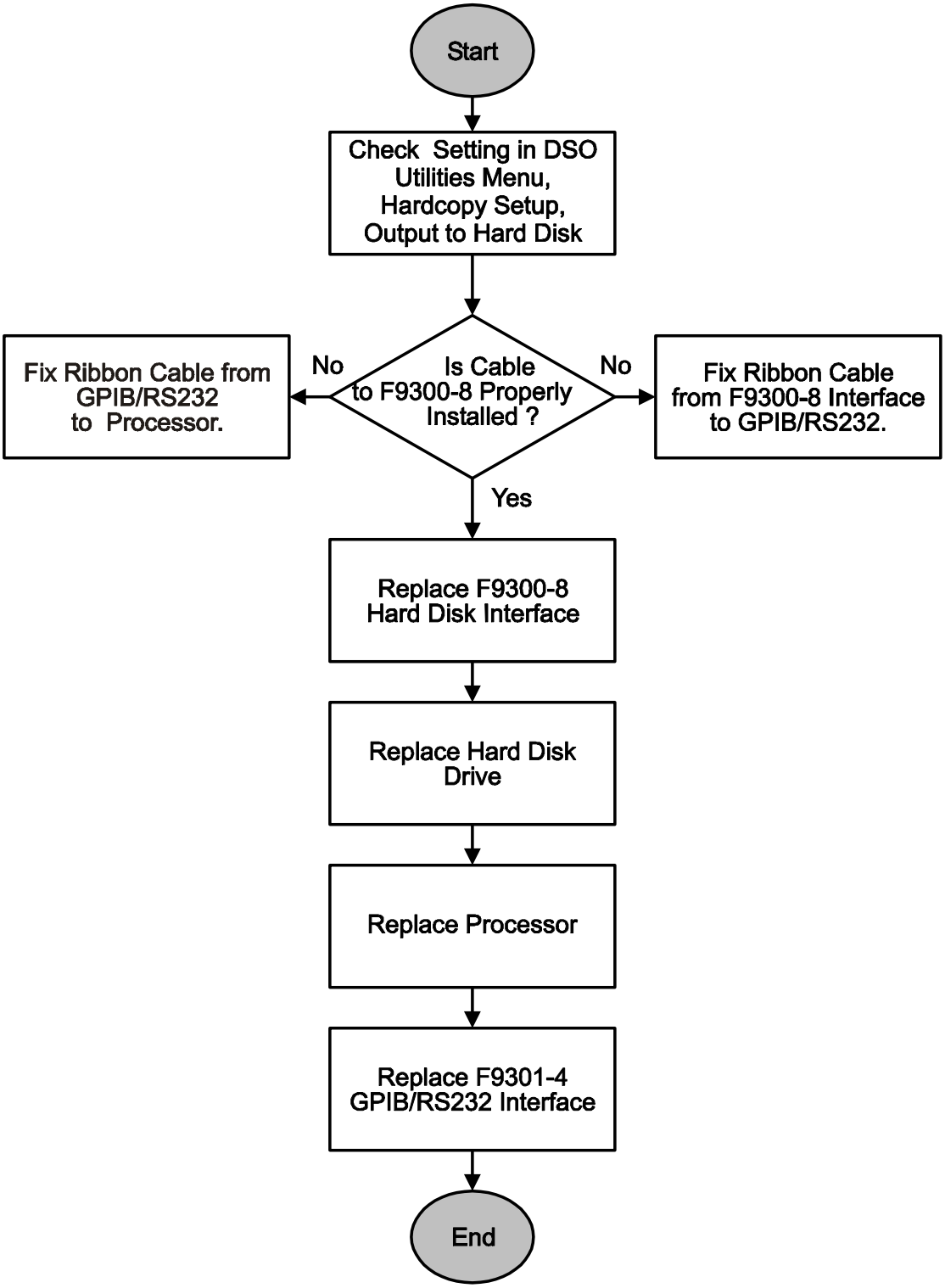
6.6.11 Graphic Printer Problem



6.6.12 Centronics Problem



6.6.13 Hard Disk Drive Problem



7. Replaceable Parts

To order parts, contact your local LeCroy service office. A list of the service centers is given in section 2 of this manual. For boards, you can either order a new board or an exchange board. Exchange assemblies are factory repaired, inspected, tested and calibrated. If you order an exchange board, you must return the defective board.

This section applies to the following model :

LC564DL

LeCroy Part Number	Description	Qty
70LC56420	LC564DL FRONT PANEL LABEL	1
LC554DL-ACC	ACCESSORIES FOR LC554DL	1
F9601-11-16	COLOR UP CARD & 2X8MB DRAM	1
900079	MAIN CARD LC564DL	1
HMM436S	*ACQUISITION MEM. MODULE 2 MBIT	16
LCDFP9615	LCD DISPLAY & FRONT PANEL ASSY	1
9615-GP01	INTERNAL GRAPHIC PRINTER	1
LCXXX-PAK	LCXXX SHIPPING AND PACKING MATERIAL	1
M9615	MECHANICAL PARTS	1
RP9615	REAR PANEL ASSEMBLY	1
UC9615	UPPER COVER ASSEMBLY	1
PS9611	300W POWER SUPPLY	1

9615-GP01: GRAPHIC PRINTER W/ TOP COVER

LeCroy Part Number	Description	Qty
334000402	THERMAL PAPER FOR SEIKO PRINTER	1
334000832	THERMAL PRINTER UNIT	1
350150001	GASKET,ULTRAFLEX,PSA,6" X 0.25"DIA	3
350920024	MONEL MESH STRIP DIAM 2.4MM	70
389340008	AUTO-ADHESIVE RUBBER BAND 12X2MM	30
530040005	SLIDE LATCH TAB STYLE	2
550010105	SCREW PAN HEAD PHIL M3X5 W/NYLOCK	7
550010106	SCREW PAN HEAD PHIL M3X6 W/NYLOCK	4
550011120	SCREW PAN HEAD PHIL M4X20 W/NYLOCK	2
551430100	FLAT WASHER M3	3
551430400	WASHER SHAKEPROOF M3	4
552430300	NUT OPEN-END ACORN M3	3
594120003	TIEWRAP	3
709450523	PUSH SWITCH EXTENDER	1
709600090	TIP-UP HANDLE	1
709601031	GRAPHIC PRINTER FRAME	1
709615006	GP01 UPPER COVER	1
70GP01041	GRAPHIC PRINTER COVER AXLE	1
70GP01051	GRAPHIC PRINTER CUTTER	1
70GP01061	GRAPHIC PRINTER SWITCH BUTTON	1
780721022	FLAT CABLE 2X10 (22CM)	1
780791604	FLAT CABLE 2X13 (4CM)	1
BOX-GP01	GP01 GRAPHIC PRINTER BOX	1
COVER-GP01	GP01 GRAPHIC PRINTER COVER	1
F9300-7	LTP 5446 PRINTER CONTROLLER	1

F9300-7: LTP 5446 PRINTER CONTROLLER

LeCroy Part Number	Description	Qty
146544471	CAP MINI ALUM 20% 470 UF	1
147494472	CAP ALU COMPACT AXIAL 4700 UF	1
190042103	RESISTOR NETWORK 10 K	1
190042472	RESISTOR NETWORK 4.7 K	2
207140007	IC QUAD STEP MOTOR DRIVER	1
208122002	IC VOLT REG POS UA7805	2
208590350	IC ADJ POWER REG 3A LM350	1
309380016	CRYSTAL OSCILLATOR (PROG) 16 MHZ	1
416161003	SWITCH PUSHBUTT ON SPST	1
430430002	RELAY 1 FORM C SPDT	1
454111002	HEADER STRAIGHT 2	1
454111006	HEADER STRAIGHT 6 PINS	1
454113003	HEADER STRAIGHT 3	1
454121003	BLOCK FOR FEM PINS 3	1
454511020	HEADER RT ANGLE MALE 20	1

F9300-7: LTP 5446 PRINTER CONTROLLER (con't)

LeCroy Part Number	Description	Qty
454511026	HDR SOLD TAIL/MALE 26	1
554435401	RIVET "RIVSCREW" M3.5	3
719300703	PC BD PREASSEMBLY 9300-7	1
CH599064012	SILICONE SEALANT RTV162	1
SM200330125	IC QUAD BUFFER 74HC125	1
SM207470175	IC QUAD DIFF LINE RECEIVER 75175	4
SM208580336	IC REF DIODE LM336-2.5V	1
SM208650393	IC DUAL VOLT COMP LM393M	1
SM227080500	IC THERM PRINTER GATE ARRAY	1
SM227090501	IC THERM PRINTER CPU	1
SM236030099	DIODE SO-PKG BAV99	8
SM270330848	TRANSISTOR NPN BC848C	2
SM652101101	RES CHIP (E24) 1% 100 OHM	12
SM652101102	RES CHIP (E24) 1% 1 K	1
SM652101103	RES CHIP (E24) 1% 10 K	26
SM652101104	RES CHIP (E24) 1% 100 K	1
SM652101132	RES CHIP (E24) 1% 1.3 K	3
SM652101151	RES CHIP (E24) 1% 150 OHM	1
SM652101162	RES CHIP (E24) 1% 1.6 K	2
SM652101201	RES CHIP (E24) 1% 200 OHM	1
SM652101223	RES CHIP (E24) 1% 22 K	1
SM652101301	RES CHIP (E24) 1% 300 OHM	3
SM652101302	RES CHIP (E24) 1% 3 K	1
SM652101303	RES CHIP (E24) 1% 30 K	1
SM652101391	RES CHIP (E24) 1% 390 OHM	1
SM652101472	RES CHIP (E24) 1% 4.7 K	4
SM652101510	RES CHIP (E24) 1% 51 OHMS	1
SM652101513	RES CHIP (E24) 1% 51 K	1
SM652101514	RES CHIP (E24) 1% 510 K	1
SM652101563	RES CHIP (E24) 1% 56 K	2
SM652101621	RES CHIP (E24) 1% 620 OHM	2
SM652101682	RES CHIP (E24) 1% 6.8 K	1
SM654101000	CHIP JUMPER ZERO OHMS	2
SM661127104	CAP CERA CHIP 20% .1 UF	2
SM661207103	CAP CERA CHIP 20% .01 UF	23
SM661255101	CAP CERA CHIP 5% 100 PF	1
SM661255471	CAP CERA CHIP 5% 470 PF	4
SM668016226	CAP,TANT 22UF/16V 20% L ESR	2

F9300-8: HD CONTROLLER

LeCroy Part Number	Description	Qty
205750000	IC GAL16V8A-15LP	2
330100100	PCMCIA HEADER ASSEMBLY TOP/LEFT	1
380450012	NR ADHESIVE TAPE 4X12 MM	6
454511040	HDR SOLD TAIL/MALE 40/RT	1
550010706	SCREW ECO-FIX PHIL PAN M3X6 W/NYLOC	4
550011106	SCREW PAN HD M2X6 BLK W/NYLOCK	4
552120100	NUT HEX M2X0.5D	4
594230002	CABLE CLIP ADHESIVE BACK	1
709300811	9300-8 PCMCIA III CONT.BRACKET	1
709300821	9300-8 PCMCIA III CONT. COVER	1
709300831	9300-8 PCMCIA III CONTR. LABEL	1
719300803	PC BD PREASS'Y 9300-8	1
CH599011002	LOCTITE SCREW LOCK GLUE	0
SM200178002	IC 2-INPUT NOR HCT02	1
SM200178374	IC D-TYP FLOP 74HCT374	2
SM201178175	IC QUAD D FLIP FLOP 74HCT175	1
SM206885245	IC BUS TRANSCVR ABT245	1
SM207170036	IC HEX BUFFER 3-STATE 74HCT365	3
SM208470358	IC DUAL OP AMP LM358D	1
SM208780109	IC MICROPOWER DC-DC CONV 1109CS8	1
SM232032814	DIODE ARRAY 2814	2
SM253030750	*DIODE HI-CUR SCHOTTKY 2HCS750	1
SM275330858	TRANSISTOR PNP BC858C	1
SM280171005	TRANSISTOR POWER MOSFET MTD10N05E	1
SM300056332	INDUCTOR WOUND 33 UH	1
SM652101102	RES CHIP (E24) 1% 1 K	3
SM652101103	RES CHIP (E24) 1% 10 K	18
SM652101104	RES CHIP (E24) 1% 100 K	1
SM652101122	RES CHIP (E24) 1% 1.2 K	1
SM652101220	RES CHIP (E24) 1% 22 OHMS	1
SM652101334	RES CHIP (E24) 1% 330 K	1
SM652101511	RES CHIP (E24) 1% 510 OHM	1
SM652101513	RES CHIP (E24) 1% 51 K	1
SM654101000	CHIP JUMPER ZERO OHMS	1
SM661207103	CAP CERA CHIP 20% .01 UF	11
SM661207104	CAP CERA CHIP 20% .1 UF	6
SM666327225	CAP MOLD TANT CHIP 2.2 UF	1
SM668016226	CAP,TANT 22UF/16V 20% L ESR	3

F9301-4: GPIB + RS232 H-SPEED INTERFACE

LeCroy Part Number	Description	Qty
116515560	CAP DIP MICA DM10 56 PF	1
405204000	JACKSCREW 3/16 HEX M/F 4-40THD	2
453521024	CONN RT ANGLE IEEE FEM 24	1
454511040	HDR SOLD TAIL/MALE 40/RT	1
455413009	CONN RT ANGL MALE 9 S-CLIP	1
550010108	SCREW PAN HEAD PHIL M3X8 W/NYLOCK	2
550010706	SCREW ECO-FIX PHIL PAN M3X6 W/NYLOC	4
709300411	GPIB-RS232 INTERFACE BRACKET	1
709300421	LABEL RS232-IEEE488-2	1
719301403	PC BD PREASS'Y 9301-4	1
SM205010401	PROGRAMMED GAL TNTSEQ-A	1
SM205010402	PROGRAMMED GAL TNTDEC-A	1
SM207180126	IC QUAD BUFFER/LINE DRIVER 3-STATE	1
SM207490232	IC XMTR/RCVR MAX 232A	1
SM207763650	IC UART 16C650	1
SM227510488	IC GPIB INTERFACE CNTRL TNT 4882	1
SM309043040	CRYSTAL OSCIL. CMOS 40 MHZ	1
SM311518432	CRYSTAL OSCI L. TTL 1.8432 MHZ	1
SM653101439	RES CHIP 1% 3.01 K	1
SM653101458	RES CHIP 1% 4.75 K	2
SM653101473	RES CHIP 1% 6.81 K	1
SM654101000	CHIP JUMPER ZERO OHMS	2
SM661207104	CAP CERA CHIP 20% .1 UF	15
SM661255221	CAP CERA CHIP 5% 220 PF	5
SM661255330	CAP CERA CHIP 5% 33 PF	16
SM666217106	CAP MOLD TANT CHIP 10 UF	1

F9601-11-16: COLOR UP CARD & 2X8MB DRAM

LeCroy Part Number	Description	Qty
205800234	*2M X 32 DRAM MODULE	2
S9601-11	COLOR PROCESS. CARD WHOUT DRAM	1

S9601-11: COLOR PROCESS. CARD WHOUT DRAM

LeCroy Part Number	Description	Qty
208591431	IC ADJ SHUNT REG TL431	1
309380016	CRYSTAL OSCILLATOR (PROG) 16 MHZ	1
312590070	BATTERY LITHIUM 3V 70MAH	1
404500068	CONN BD TO BD 68 POS	1
453250072	CONN PC EDGE/SOLD TAIL 72	2
454110026	HDR SOLD TAIL MALE 26 ST	1
454110040	HDR SOLD TAIL/MALE 40/STRAIGHT	2
454110120	HDR SOLD TAIL/MALE 20/STRAIGHT	2
454111050	HDR SOLD TAIL/MALE 50/STRAIGHT	1
454312010	HDR SOLD TAIL/MALE 10	1
454314016	HDR SOLD TAIL/MALE 16	2
455410096	CONN RT ANGL MALE 96 S-CLIP	1
505322001	HEATSINK FOR PGA 11X11	1
591002130	WIRE TEF BLK SOLID AWG 30	3
719601103H	PC BD PREASS'Y 9601-11	1
CH599045013	THERMALLY CONDUCTIVE ADHESIVE	0
SM200172138	IC 3 TO 8 DECODER 74F138	2
SM200178002	IC 2-INPUT NOR HCT02	1
SM200178004	IC HEX INVERTER HCT04	1
SM200178086	IC 2-IN EXCL-OR HCT86	2
SM200178139	IC 2-TO-4-LINE DECODER HCT139	1
SM200178374	IC D-TYP FLOP 74HCT374	2
SM200276068	IC RTC SERIAL 68HC68T1	1
SM200278040	IC COUNTER HCT4040	1
SM200278390	IC 4-BIT RIPPLE COUNTER 74HCT390	1
SM200344174	IC HEX D-FLOP HCT 174	1
SM205144001	IC 8-MBIT FLASH MEM 28F008SA	2
SM205219256	IC 32K X 8 SRAM MS62256	1
SM205244260	IC 256K X 16 DRAM MCM54260	2
SM205721002	PROGRAMMED GAL 16V8D-15 RAMEUR D	1
SM205921003	PROGRAMMED GAL BUDGET-D	1
SM205921004	PROGRAMMED GAL CARDAN-B	1
SM205921005	PROGRAMMED GAL DRAMES-C	1
SM205921006	PROGRAMMED GAL GRANDS-B	1
SM205921007	PROGRAMMED GAL OCCASE-B	1
SM205921008	PROGRAMMED GAL PETITS-C	1
SM205921009	PROGRAMMED GAL PROFIL-B	1
SM205921011	PROGRAMMED GAL RASADE-B	1
SM205921012	PROGRAMMED GAL RETINE-C	1
SM205921013	PROGRAMMED GAL SAVEUR-B	1
SM205921014	PROGRAMMED GAL SEVERE-B	1
SM205921015	PROGRAMMED GAL VIADUC-B	1
SM205921019	PROGRAMMED GAL ASSISE-F	1
SM207170036	IC HEX BUFFER 3-STATE 74HCT365	3
SM207178541	IC BUFFER/LINE DR HCT541	7

S9601-11: COLOR PROCESS. CARD WHOUT DRAM (con't)

LeCroy Part Number	Description	Qty
SM207179244	IC BUFFER/LINE DRIV HCT244	1
SM207660150	IC DYNAMIC BUS SIZER MC68150	1
SM207665545	IC FLAT PANEL VGA CONTROLLER	1
SM207878245	IC BUS TRANSCVR HCT245	3
SM207972157	IC DATA SEL/MUX 74F157A	4
SM208470358	IC DUAL OP AMP LM358D	2
SM208680916	IC LOW SKEW CLOCK DRIVER 88916	1
SM208780109	IC MICROPOWER DC-DC CONV 1109CS8	1
SM227063201	IC IBM/PC FLOPPY DISK CONTROLLER	1
SM227300059	IC INTERRUPT CONTROLLER UPD71059	1
SM227300603	IC RISC PROCESSOR MPC603E	1
SM227870695	MICRO-PROC PWR SUPVR	1
SM236030099	DIODE SO-PKG BAV99	3
SM253030750	*DIODE HI-CUR SCHOTTKY 2HCS750	1
SM253032823	DIODE SCHOTTKY 2823	1
SM256232013	DIODE LIGHT EMITTING RED	1
SM270130092	TRANSISTOR NPN BFR92A	1
SM270330848	TRANSISTOR NPN BC848C	1
SM280071048	TRANS DMOSFET N-CH TN0104N8	1
SM280171005	TRANSISTOR POWER MOSFET MTD10N05E	2
SM290101020	TTL DELAY LINE, 5 X 4NS/TAP	2
SM300056332	INDUCTOR WOUND 33 UH	1
SM300327102	INDUCTOR WOUND 1 UH	1
SM301502001	BEAD (FERRITE CHIP)	3
SM310300406	CRYSTAL 32768 HZ	1
SM310900024	CRYSTAL 24 MHZ SMD	1
SM652101100	RES CHIP (E24) 1% 10 OHMS	3
SM652101101	RES CHIP (E24) 1% 100 OHM	29
SM652101102	RES CHIP (E24) 1% 1 K	56
SM652101103	RES CHIP (E24) 1% 10 K	34
SM652101104	RES CHIP (E24) 1% 100 K	4
SM652101106	RES CHIP (E24) 5% 10 M	2
SM652101122	RES CHIP (E24) 1% 1.2 K	1
SM652101150	RES CHIP (E24) 1% 15 OHMS	1
SM652101151	RES CHIP (E24) 1% 150 OHM	5
SM652101153	RES CHIP (E24) 1% 15 K	2
SM652101154	RES CHIP (E24) 1% 150 K	2
SM652101220	RES CHIP (E24) 1% 22 OHMS	29
SM652101241	RES CHIP (E24) 1% 240 OHM	1
SM652101242	RES CHIP (E24) 1% 2.4 K	2
SM652101331	RES CHIP (E24) 1% 330 OHM	1
SM652101470	RES CHIP (E24) 1% 47 OHMS	2
SM652101472	RES CHIP (E24) 1% 4.7 K	33
SM652101474	RES CHIP (E24) 1% 470 K	1
SM652101510	RES CHIP (E24) 1% 51 OHMS	9
SM652101511	RES CHIP (E24) 1% 510 OHM	9

S9601-11: COLOR PROCESS. CARD WHOUT DRAM (con't)

LeCroy Part Number	Description	Qty
SM652101512	RES CHIP (E24) 1% 5.1 K	1
SM652101752	RES CHIP (E24) 1% 7.5 K	1
SM652101820	RES CHIP (E24) 1% 82 OHMS	6
SM654101000	CHIP JUMPER ZERO OHMS	11
SM661207102	CAP CERA CHIP 20% .001 UF	2
SM661207103	CAP CERA CHIP 20% .01 UF	105
SM661207104	CAP CERA CHIP 20% .1 UF	6
SM661255100	CAP CERA CHIP 5% 10 PF	2
SM661255101	CAP CERA CHIP 5% 100 PF	4
SM661255180	CAP CERA CHIP 5% 18 PF	2
SM661255221	CAP CERA CHIP 5% 220 PF	2
SM666217106	CAP MOLD TANT CHIP 10 UF	2
SM666237476	CAP MOLD TANT CHIP 47 UF	8
SM666327225	CAP MOLD TANT CHIP 2.2 UF	2
SM668016476	CAP, TANT 47UF/16V 20% LOW ESR	1

F9601-2: CENTRONICS AND VGA INTERFACE

LeCroy Part Number	Description	Qty
405204000	JACKSCREW 3/16 HEX M/F 4-40THD	6
454110040	HDR SOLD TAIL/MALE 40/STRAIGHT	1
454520025	CONN RT ANGLE FEM 25 S-CLIP	1
454630015	CONN FEM SUBMINIATURE D-15	2
550010706	SCREW ECO-FIX PHIL PAN M3X6 W/NYLOC	2
709601211	9601-2 BRACKET	1
719601203	PC BD PREASS'Y 9601-2	1
SM253032823	DIODE SCHOTTKY 2823	4
SM270330848	TRANSISTOR NPN BC848C	3
SM301502001	BEAD (FERRITE CHIP)	6
SM653101269	RES CHIP 1% 51.1 OHMS	5
SM653101285	RES CHIP 1% 75.0 OHMS	3
SM653101393	RES CHIP 1% 1.00 K	3
SM653101439	RES CHIP 1% 3.01 K	6
SM653101522	RES CHIP 1% 22.1 K	2
SM661207104	CAP CERA CHIP 20% .1 UF	1
SM661255470	CAP CERA CHIP 5% 47 PF	19
SM661255471	CAP CERA CHIP 5% 470 PF	2

F9601-61: FLOPPY DISK DRIVE ASSY

LeCroy Part Number	Description	Qty
330000002	3.5" DISC DRIVE, 0.44" HIGH	1
453411026	CONN ZIF FOR FFC 26 POS	1
454110026	HDR SOLD TAIL MALE 26 ST	1
550010103	SCREW PAN HEAD PHIL M2.5X3 W/NYLOCK	4
550010706	SCREW ECO-FIX PHIL PAN M3X6 W/NYLOC	2
709600611	FLOPPY DRIVE SUPPORT	1
719601603	PC BD PREASS'Y FOR 9601-6	1
780919905	FLAT FLEX CABLE 26 P. 5CM	1

F9601-8: MAIN SWITCH BOARD

LeCroy Part Number	Description	Qty
161445105	RES CARBON FILM 1 MEG	1
416121004	MAIN POWER SWITCH	1
454115103	HDR FRICTION LOCK 3X1-PIN	3
719601803	PC BD PREASS'Y FOR 9601-8	1

F9602-9: FAN UNIVERSAL CONTROL. ASSY.

LeCroy Part Number	Description	Qty
169416223	RESISTOR DISC NTC 22 K	1
405154002	CONN HOUSING 2-POS	1
405708001	TERMINAL ANTI-FISHHOOKING CRIMP	2
530409116	12V DC FAN, BRUSHLESS	1
554010013	SCREW S/TAP PAN HD M3.5X13	2
554035101	CLIP-ON NUT DIAM. 3.5	2
590001022	WIRE TEFLON 7/30 BLK 22	1
590221022	WIRE TEFLON 7/30 RED 22	1
S9602-9	FAN UNIVERSAL CONTROL. CIRCUIT	1

900079: MAIN CARD LC554DL

LeCroy Part Number	Description	Qty
SM454213056	Conn CIN:APSE 56 Pts 3.5MM	4
SM454213064	Conn CIN:APSE 64 Pts 3.5MM	4
709614315	HAM421 Tightener	8
709614321	HAM421 Heatsink	4
709614301	BNC Lock Washer	6
709614302	BNC Nut	6
S9615-3	Main Card Quad 4 Ghz	1
554422006	Screw S/Tap Pan Phil KA22X5	2
554425003	Screw S/Tap Phil M2.5X6 Black	6
7093XXP41	Probe Holder	6
7093XXP91	Probe Ring Contact	6
709600020	9600 Right Hub Cap	1
709600024	9600 Left Hub Cap	1
552420100	4MM Hex Nut M2 Thd	8
205800234	2M X 32 Dram Module	2
HAM435	2GS/S Acq. Module	4
FP9615-3	Main Card Panel 9615-3	1
550420110	Screw Cyl HD Phil M2X10MM	8
551420400	Washer Shakeproof M2	33
CH599041022	Heat Sink Compound 251	1.45
709614312	HSY 425 Tightener	8
SM454213016	Conn CIN:APSE 16 Pts 1.4MM	8
HSY430	Switch Yard Board HSY430	2
550120116	Screw Pan HD PH M2X16 ST Stl P	1
550120104	Screw Pan HD HP M2X4 ST Stl PA	1
350351001	Gasket, Shielding, Clip-ON	0.0625
550420820	Screw Cyl HD Phil M2X20	15

S9615-3: BASE MAIN CARD

LeCroy Part Number	Description	Qty
145344109	CAP ALU COMPACT AXIAL 10000UF	1
168904651	RES ULTRA PREC 487K 0.25%	1
169416473	RESISTOR DISC NTC 47 K	1
208123002	IC +12 VOLT REG LM340T-12	2
208124003	IC VOLT REG -12V LM320T-12	2
208570317	IC ADJ +V REG LM317	1
208700001	IC VCO TUNABLE FROM 1350 TO 2400MHZ	1
281194905	P CH POWER MOSFET IRF4905	1
404531112	CON EDGE PCI LOW PROFILE 112P	16
405812006	H/PROFL SOCKET STRIP 12 POS	1
430430004	RELAY HF 12V MINIATURE	2
430500003	20DB ATTENUATOR RELAY DC-3GHZ	4
453150072	CONN PC EDGE/SOLD REFLOW 72	2
454220096	HDR PRESSFIT TO FEM 96	1
455410011	POWER CONNECTOR 11 POS. 25A	1
505052002	HEAT SINK HORIZ MTG TO-220	5
505072001	HEATSINK TO-220 VERT MNT	1
505322001	HEATSINK FOR PGA 11X11	2
555000220	SPRING FOR SK129 HEATSINK	1
709360371	HEATSINK	2
7093XXP01	RIGHT ANGLE RECEPT. CONNECTOR	6
709614300	BULKHEAD RECEPTICAL FEMALE BNC	6
709614330	HFE428 HEATSINK	9
709614331	HFE428 HEATSINK CLIP	9
71961530D	PC BD PREASSY 9615-3	1
CH599041022	HEAT SINK COMPOUND 251	0
CH599045013	THERMALLY CONDUCTIVE ADHESIVE	0
CH599064012	SILICONE SEALANT RTV162	0
HFE444	HYBRID DSO FRONT END 1GHZ	4
HTR420	CHIP ON BOARD ASSY HTR420	5
MCG426	IC CLOCK GENERATOR GATE-ARRAY	1
MNX427	IC MINMAX GATE ARRAY	4
MST429A	*IC SMART TRIGGER GATE-ARRAY	1
MTB411A	MONOLITHIC TIME BASE	1
SM158240200	CAP VARIABLE .6 - 2.5 PF	1
SM158240201	CAP VARIABLE 1 - 5 PF	8
SM158240202	CAP VARIABLE 2.5 - 10 PF	5
SM168651008	RES METAL FILM 1% 100 OHM	10
SM168651326	RES METAL FILM 1% 200 OHM	1
SM168659004	RES METAL FILM .1% 900 OHMS	1
SM168659007	RES METAL FILM .1% 3.00K	4
SM168659297	RES METAL FILM .1% 100 OHMS	3
SM185457102	RES VARI CERMET 1 K	4
SM185457103	RES VARI CERMET 10 K	5
SM185457201	RES VARI CERMET 200 OHMS	1
SM185457503	RES VARI CERMET 50 K	4

S9615-3: BASE MAIN CARD

LeCroy Part Number	Description	Qty
SM200178000	IC 2-INPUT NAND HCT00	1
SM200178002	IC 2-INPUT NOR HCT02	2
SM200178030	IC 8-IN NAND HCT30	1
SM200178074	IC D-TYP FLOP 74HCT74	5
SM200178138	IC 3-TO-8-LINE DECODER HCT138	2
SM200178139	IC 2-TO-4-LINE DECODER HCT139	1
SM200178273	IC D-TYP FLOP 74HCT273	1
SM200330125	IC QUAD BUFFER 74HC125	1
SM201174011	IC ECL 1:2 DIFF CLOCK DRVR 10EL11D	4
SM201174051	IC ECL DIFF CLOCK FLIP FLOP 10EL51D	1
SM201177032	IC 4X2 INPUT OR 74ACT32	16
SM201274033	IC ECL DIVIDE BY 4 MC10EL33	3
SM201570016	IC ECL DIFF RECEIVER 10EL16D	5
SM205108016	IC EEPROM 16K BIT IIC BUS	2
SM205238256	IC 32K X 8 SRAM 25NS	1
SM205618165	IC 8-BIT SHIFT REG 74HCT165	3
SM205618594	IC 8-BIT SHIFT REG 74HC594	10
SM205913125	*FPGA ISPLSI 1048E-125LQ	2
SM205921301	PROGRAMMED GAL SWATCH-B	1
SM206070584	IC BUS CONTROLLER 8584	1
SM206260858	IC OCT 8-BIT ADC SYSTEM 858	1
SM206885245	IC BUS TRANSCVR ABT245	2
SM207170036	IC HEX BUFFER 3-STATE 74HCT365	5
SM207171244	IC OCTAL BUFFER ABT244	2
SM207200549	*DUAL 8-BIT DAC MAX549	4
SM207247610	DAC,OCTAL 14-BIT,SER ACCESS	3
SM207288800	IC OCTL 8-BIT CMOS D/A CONV DAC8800	2
SM207360124	IC TRANSLATOR MC10124	2
SM207360125	IC TRANSLATOR MC10125	1
SM207770403	IC ANALOG SWITCH DG403	1
SM207770442	IC ANALOG SWITCH DG442	5
SM207880245	IC OCTAL BI-DIR BUFFER 3.3V	8
SM207970351	IC OCTAL ANALOG MUX/DEMUX 74HC4351	1
SM207978153	IC 4-INPUT MUX HCT153	1
SM207978251	IC 8-IN MUX 3-ST 74HCT251	2
SM208030245	IC TRANS ARRAY NPNX6 SL3245	1
SM208450686	IC WIDEBAND OP AMP OPA686	4
SM208470027	IC SINGLE OP AMP OP-27	2
SM208470037	IC OP AMP 37GS	1
SM208470324	IC OP AMP LM324M	5
SM208470353	IC DUAL OP AMP LF353	2
SM208470358	IC DUAL OP AMP LM358D	11
SM208470705	IC OP AMP PICOAMP INPUT AD705	13
SM208474005	FET-INPUT BUFFER MAX4005	1
SM208476172	DUAL HIGH SPEED OP AMP	1

S9615-3: BASE MAIN CARD

LeCroy Part Number	Description	Qty
SM208480660	IC OP AMP OPA660	4
SM208570078	IC LOW POWER REG +12V 78L12	4
SM208570805	IC POS VOLT REG 78L05	2
SM208570905	IC NEG VOLT REG 79L05	1
SM208591336	IC VOLT REF DIODE LM336	12
SM208701023	IC TEMPERATURE SENSOR	16
SM208870339	IC VOLT COMPARATOR 339	6
SM208880079	IC LOW POW REG -12V 79L12	4
SM208909850	DDS-125MHZ CMOS SYNTH AD9850	1
SM208974881	VIDEO SYNC SEPARATOR GS4881	1
SM229020150	MLC TRANS VOLT SUPPRESSOR	6
SM232022822	DIODE ARRAY SCHOTTKY 2822	6
SM232022824	DIODE ARRAY SCHOTTKY HSMS2824	2
SM232120070	DIODE ARRAY BAV70	2
SM236030099	DIODE SO-PKG BAV99	24
SM240050051	DIODE ZENER TZM-C-5V1	1
SM240218451	DIODE ZENER BZX84C5V1	1
SM240218462	DIODE ZENER BZX84C6V2	4
SM240218475	DIODE ZENER BZX84C7V5	2
SM252005303	PIN DIODE BAR 63-03W	16
SM252005305	PIN DOIDE BAR 63-05W	8
SM252023066	PIN DIODE BAR 66	16
SM252023304	DUAL PIN DIODE SILICON BAR 63-04	5
SM252023306	DUAL PIN DIODE SILICON BAR 63-06	1
SM252080682	DIODE PIN BA682	7
SM253032823	DIODE SCHOTTKY 2823	1
SM253260060	SHOTTKY DIODE, SIL BAT60B	4
SM270050520	NPN 9GHZ WIDEBAND TRANSISTOR	12
SM270080868	TRANSISTOR NPN BC868	2
SM270130092	TRANSISTOR NPN BFR92A	12
SM270330848	TRANSISTOR NPN BC848C	4
SM270650182	NPN RF TRANSISTOR BFP182W	8
SM270690799	NPN RF TRANSISTOR BF 799W	4
SM275030550	TRANSISTOR PNP BF550	14
SM275330858	TRANSISTOR PNP BC858C	2
SM280071048	TRANS DMOSFET N-CH TN0104N8	1
SM280120605	LOW POWER NMOSFET	21
SM280122416	TRANS. JFET N MMBF4416/LC6A	4
SM280171005	TRANSISTOR POWER MOSFET MTD10N05E	7
SM281120610	LOW POWER PMOSFET TRANSISTOR	5
SM289772003	TRANSISTOR ARRAY 2003	4
SM300000103	INDUCTOR 10UH 30% 0805	4
SM300097392	SMD POWER INDUCTOR 3.9UH 15A	1
SM300306100	INDUCTOR CHIP 10% 10NH	1
SM300396220	INDUCTOR CHIP 10% 220NH 0805	4
SM301502001	BEAD (FERRITE CHIP)	42

S9615-3: BASE MAIN CARD

LeCroy Part Number	Description	Qty
SM311210254	CRYSTAL OSC 2.5PPM 10MHZ	1
SM402122001	CONN CO-AX PC MTG MMCX	9
SM411151010	DIP SWITCH SMD 10XSPST	1
SM430530001	RELAY SMD DUAL FORM C 5V	16
SM430710008	RELAY SMD REED MRF-8	8
SM455710008	SMT JACK CONNECTOR 8 CONTACTS	1
SM530040001	BUZZER 90DB 4-7V SMD	1
SM651081102	RES CHIP 0.1% 1 KOHM	4
SM651104151	RES CHIP 1% 25PPM 150 OHMS	1
SM651104182	RES CHIP 1% 25PPM 1.8K	1
SM651104183	RES CHIP 1% 25PPM 18 K	1
SM651104201	RES CHIP 1% 25PPM 200 OHM	1
SM651104204	RES CHIP 1% 25PPM 200 K	1
SM651104392	RES CHIP 1% 25PPM 3.9K	1
SM651352184	*RES CHIP .25% 180K	4
SM651452824	*RES CHIP .25% 820K	4
SM651452914	*RES CHIP .25% 910K 150V	4
SM652061000	RES CHIP 0 OHM JUMPER	4
SM652061100	RES CHIP 1% 10.0 OHM .063W	4
SM652061101	RES CHIP 1% 100 OHM .063W	28
SM652061102	RES CHIP 1% 1.0K OHM .063W	12
SM652061103	RES CHIP 1% 10K OHM .063W	56
SM652061104	RES CHIP 1% 100K OHM .063W	28
SM652061105	RES CHIP 1% 1.0M OHM .063W	12
SM652061106	RES CHIP 1% 10M OHM .063W	4
SM652061122	RES CHIP 1% 1.2K OHM .063W	4
SM652061124	RES CHIP 1% 120K OHM .063W	8
SM652061133	RES CHIP 1% 13K OHM .063W	4
SM652061151	RES CHIP 1% 150 OHM .063W	8
SM652061154	RES CHIP 1% 150K OHM .063W	4
SM652061201	RES CHIP 1% 200 OHM .063W	8
SM652061202	RES CHIP 1% 2.0K OHM .063W	8
SM652061205	RES CHIP (E24) 1% 2.0M	4
SM652061221	RES CHIP 1% 220 OHM .063W	12
SM652061240	RES CHIP 1% 24.0 OHM .063W	12
SM652061244	RES CHIP 1% 240K OHM .063W	4
SM652061272	RES CHIP 1% 2.7K OHM .063W	8
SM652061273	RES CHIP 1% 27K OHM .063W	4
SM652061304	RES CHIP 1% 300K OHM .063W	8
SM652061332	RES CHIP 1% 3.3K OHM .063W	4
SM652061333	RES CHIP 1% 33K OHM .063W	4
SM652061334	RES CHIP 1% 330K OHM .063W	4
SM652061361	RES CHIP 1% 360 OHM .063W	20
SM652061390	RES CHIP 1% 39.0 OHM .063W	4
SM652061393	RES CHIP 1% 39K OHM .063W	4

S9615-3: BASE MAIN CARD

LeCroy Part Number	Description	Qty
SM652061431	RES CHIP 1% 430 OHM .063W	8
SM652061470	RES CHIP 1% 47.0 OHM .063W	4
SM652061471	RES CHIP 1% 470 OHM .063W	4
SM652061472	RES CHIP 1% 4.7K OHM .063W	20
SM652061510	RES CHIP 1% 51.0 OHM .063W	17
SM652061511	RES CHIP 1% 510 OHM .063W	4
SM652061513	RES CHIP 1% 51K OHM .063W	4
SM652061515	RES CHIP (E24) 1% 5.1M	4
SM652061562	RES CHIP 1% 5.6K OHM .063W	4
SM652061563	RES CHIP 1% 56K OHM .063W	4
SM652061682	RES CHIP 1% 6.8K OHM .063W	4
SM652061752	RES CHIP 1% 7.5K OHM .063W	12
SM652061822	RES CHIP 1% 8.2K OHM .063W	4
SM652061824	RES CHIP 1% 820K OHM .063W	4
SM652069393	RES CHIP (E24) .1% 39K	8
SM652101100	RES CHIP (E24) 1% 10 OHMS	5
SM652101101	RES CHIP (E24) 1% 100 OHM	73
SM652101102	RES CHIP (E24) 1% 1 K	54
SM652101103	RES CHIP (E24) 1% 10 K	148
SM652101104	RES CHIP (E24) 1% 100 K	3
SM652101105	RES CHIP (E24) 1% 1 M	1
SM652101112	RES CHIP (E24) 1% 1.1 K	6
SM652101121	RES CHIP (E24) 1% 120 OHM	10
SM652101122	RES CHIP (E24) 1% 1.2 K	4
SM652101123	RES CHIP (E24) 1% 12 K	1
SM652101124	RES CHIP (E24) 1% 120 K	1
SM652101131	RES CHIP (E24) 1% 130 OHM	4
SM652101132	RES CHIP (E24) 1% 1.3 K	1
SM652101150	RES CHIP (E24) 1% 15 OHMS	1
SM652101151	RES CHIP (E24) 1% 150 OHM	1
SM652101152	RES CHIP (E24) 1% 1.5 K	5
SM652101154	RES CHIP (E24) 1% 150 K	1
SM652101162	RES CHIP (E24) 1% 1.6 K	1
SM652101181	RES CHIP (E24) 1% 180 OHM	2
SM652101182	RES CHIP (E24) 1% 1.8 K	4
SM652101183	RES CHIP (E24) 1% 18 K	7
SM652101201	RES CHIP (E24) 1% 200 OHM	65
SM652101202	RES CHIP (E24) 1% 2 K	12
SM652101203	RES CHIP (E24) 1% 20 K	1
SM652101204	RES CHIP (E24) 1% 200 K	1
SM652101220	RES CHIP (E24) 1% 22 OHMS	47
SM652101221	RES CHIP (E24) 1% 220 OHM	1
SM652101222	RES CHIP (E24) 1% 2.2 K	7
SM652101223	RES CHIP (E24) 1% 22 K	1
SM652101240	RES CHIP (E24) 1% 24 OHMS	4
SM652101241	RES CHIP (E24) 1% 240 OHM	1

S9615-3: BASE MAIN CARD

LeCroy Part Number	Description	Qty
SM652101243	RES CHIP (E24) 1% 24 K	1
SM652101271	RES CHIP (E24) 1% 270 OHM	3
SM652101273	RES CHIP (E24) 1% 27 K	1
SM652101301	RES CHIP (E24) 1% 300 OHM	5
SM652101302	RES CHIP (E24) 1% 3 K	1
SM652101304	RES CHIP (E24) 1% 300 K	4
SM652101330	RES CHIP (E24) 1% 33 OHMS	12
SM652101331	RES CHIP (E24) 1% 330 OHM	3
SM652101332	RES CHIP (E24) 1% 3.3 K	11
SM652101333	RES CHIP (E24) 1% 33 K	1
SM652101360	RES CHIP (E24) 1% 36 OHM	1
SM652101391	RES CHIP (E24) 1% 390 OHM	16
SM652101392	RES CHIP (E24) 1% 3.9 K	1
SM652101394	RES CHIP (E24) 1% 390 K	1
SM652101430	RES CHIP (E24) 1% 43 OHMS	18
SM652101434	RES CHIP (E24) 1% 430 K	1
SM652101471	RES CHIP (E24) 1% 470 OHM	16
SM652101472	RES CHIP (E24) 1% 4.7 K	1
SM652101510	RES CHIP (E24) 1% 51 OHMS	33
SM652101511	RES CHIP (E24) 1% 510 OHM	3
SM652101512	RES CHIP (E24) 1% 5.1 K	12
SM652101514	RES CHIP (E24) 1% 510 K	1
SM652101561	RES CHIP (E24) 1% 560 OHM	10
SM652101562	RES CHIP (E24) 1% 5.6 K	4
SM652101620	RES CHIP (E24) 1% 62 OHMS	29
SM652101621	RES CHIP (E24) 1% 620 OHM	1
SM652101624	RES CHIP (E24) 1% 620 K	1
SM652101681	RES CHIP (E24) 1% 680 OHM	4
SM652101683	RES CHIP (E24) 1% 68 K	4
SM652101684	RES CHIP (E24) 1% 680 K	1
SM652101750	RES CHIP (E24) 1% 75 OHMS	44
SM652101751	RES CHIP (E24) 1% 750 OHM	4
SM652101752	RES CHIP (E24) 1% 7.5 K	2
SM652101820	RES CHIP (E24) 1% 82 OHMS	4
SM652101824	RES CHIP (E24) 1% 820 K	2
SM652101911	RES CHIP (E24) 1% 910 OHM	2
SM652101914	RES CHIP (E24) 1% 910 K	4
SM654101000	CHIP JUMPER ZERO OHMS	30
SM661028100	CAP CERA CHIP 1UF 10V	8
SM661066102	CAP CERA CHIP 10% 1000PF/50V	136
SM661068104	CHIP CERAMIC CAPACITOR	72
SM661073010	CAP CERA 1.0 +/-0.1PF 50V NPO	4
SM661073331	CAP CERA 330PF+/- 5% 50V NPO	4
SM661073820	CAP CERA 82PF+/- 5% 50V NPO	4
SM661205682	CAP CERA CHIP 5% 6800 PF	2

S9615-3: BASE MAIN CARD

LeCroy Part Number	Description	Qty
SM661207102	CAP CERA CHIP 20% .001 UF	20
SM661207103	CAP CERA CHIP 20% .01 UF	303
SM661207104	CAP CERA CHIP 20% .1 UF	135
SM661207223	CAP CERA CHIP 20% .022 UF	4
SM661251022	CAP CERA CHIP 2.2PF +/-.1PF	4
SM661251681	CAP CERA CHIP 680PF +/-1% 50V	2
SM661255100	CAP CERA CHIP 5% 10 PF	1
SM661255101	CAP CERA CHIP 5% 100 PF	1
SM661255121	CAP CERA CHIP 5% 120 PF	2
SM661255181	CAP CERA CHIP 5% 180 PF	1
SM661255220	CAP CERA CHIP 5% 22 PF	1
SM661255470	CAP CERA CHIP 5% 47 PF	5
SM661255471	CAP CERA CHIP 5% 470 PF	16
SM661255560	CAP CERA CHIP 5% 56 PF	1
SM661256120	CAP CERA CHIP 10% 12 PF	1
SM661515102	CAP CERA CHIP 5% 1000PF 200V	4
SM661540056	CAP CERA CHIP 5.6PF 500V	1
SM661540068	CAP CERA CHIP 6.8PF 500V	1
SM661542120	CAP CERA 2% 12PF/500V NPO	1
SM667010156	CAP,TANT 15UF/10V 20%	5
SM668010335	CAP,TANT 3.3UF/10V 20% L/ESR	26
SM668010336	CAP, TANT 33UF/10V 20% L ESR	2
SM668010685	CAP,TANT 6.8UF/10V 20% L/ESR	6
SM668016476	CAP, TANT 47UF/16V 20% LOW ESR	8
SM668025334	CAP,TANT .33UF/25V 20% L/ESR	27
SM668025336	CAP,TANT 33UF/25V 20% L ESR	20
SM669080181	CHIP FERRITE BEAD	28
TCOIL9615B	PCB, PREASSY, TCOIL 9615-3	4

F9615-5: KEYBOARD ASSY

LeCroy Part Number	Description	Qty
551423100	FLAT WASHER M2.3	5
554422005	SCREW S/TAP PAN PHIL KA22X6	5
709600510	9600-5 SWITCH CAP, LIGHT GREY	32
709600512	9600-5 SWITCH CAP DARK GREY	12
709600514	9600-5 SWITCH CAP, BLUE	1
709600516	9600-5 SWITCH CAP, GREEN	1
709615500	TFT RUBBER MAT	1
709615512	FRONT PANEL CLASSIC	1
S9615-51	KEYPAD	1

LC554DL-ACC: ACCESSORIES FOR LC554DL

LeCroy Part Number	Description	Qty
433162630	Fuse Slo-Blo 250V 6.30AMP	2
597940014	Plastic Bag For 94XX 93XX	1
LCXXX-RM-E	Remote Cntrl Manual For Lcxxx	1
LCXXX-OM-E	Lcxxx Operators Manual Eng	1
LCXXX-HG-E	Hands ON Guide For Lcxxx Scope	1
LCXXX-WP03-OM-E	Statist. Analys. Pack. Manual	1
709600015	Lcxxx Protective Cover	1
709615010	Logo Lecroy For Flat Panel	1
LCXXX-AD-564	LC OM Addendum LC564 LC554	1
GENCARD	REGISTRATION CARDS	1
GENCORD	POWERCORDS FROM ACC BOMS	1
GENMANUAL	MANUALS	1
LCXXX-CECERT-E	Declaration of Conformity Eng.	1
730000301	DSO Manual Holder Inner Box	1
730000302	DSO Manual Holder Outer Box	1
PP005A	500 MHz /10 10 M Ohms CATII	4

LCDFP9615: LCD DISPLAY & FRONT PANEL ASSY

LeCroy Part Number	Description	Qty
258104001	TFT COLOR LCD MODULE, 10.4 INCH	1
300070000	FERRITE SHIELDING FLAT CABLE	1
315000003	TFT DC-AC INVERTER UNIT	1
520200120	SPACER 4MMODX2.6MMIDX5MMLG NYLON BK	2
550420108	SCREW PAN HD PHIL M2.0X8MM LG	2
550430608	*SCREW ECO-FIX M3X8	4
550430706	SCREW ECO-FIX M3X6	3
551090001	M9 LOCKWASHER	4
552090075	M9 X 0.75 MOUNTING NUT	4
592000032	FLAT CABLE 32 POS .5 STEP	1
709600560	9600-5 KNOB DIAM 9	7
709600570	9600-5 KNOB DIAM 12	4
709615007	FRONT FRAME (SHARP)	1
780684002	FLAT CABLE 5 POS	1
F9601-61	FLOPPY DISK DRIVE ASSY	1
F9615-5	KEYBOARD ASSY	1
S9615-21	BUFFER BOARD	1
S9615-22	INTERFACE CIRCUIT	1
S9615-52	GENERIC FRONT PANEL	1

LCLC9615: LOWER COVER WITH FEET

LeCroy Part Number	Description	Qty
485325001	SET OF 4 FEET, DARK GREY	1
554435006	SCREW S/TAP PAN PHIL KA35X7	8
709615305	LOWER COVER	1

LCXXX-PAK: LCXXX SHIPPING AND PACKING MATERIAL

LeCroy Part Number	Description	Qty
597574011	ACCESSORY CARTON W/URETHANE INSERT	1
597574012	PE FOAM END-CAPS(PAIR) FOR LCXXX	1
597574013	MASTER CARTON FOR LCXXX SHIPPING	1
700101100	LABEL, OSCILLOSCOPE BOX	1

M9615: MECHANICAL PARTS

LeCroy Part Number	Description	Qty
550010130	SCREW PAN HEAD PHIL M3X30 W/NYLOCK	12
550431104	SCR PN HD PH W/WHR M3X4 W/NYLOCK	2
550431106	SCR PN HD PH W/WHR M3X6 W/NYLOCK	54
550450116	SCREW CYL HD PHIL M5X16MM	4
554425003	SCREW S/TAP PHIL M2.5X6 BLACK	6
594230002	CABLE CLIP ADHESIVE BACK	3
709424096	MEMORY CARD INSERT	1
709600048	9600 UPPER COVER LOCK INSERT	2
709600075	9600 REAR FOOT	4
709600078	REAR FOOT RUBBER	4
709614340	9614 SHIELD LOWER PARTITION	6
709614800	PS SQUARE ANGLE SUPPORT	1
709615000	BEZEL CLASSIC	1
709615201	ANTIGLARE GLASS SCREEN	1
709615901	FAN CHAMBER	1
780684001	FLAT CABLE 2X25 46CM	1
780721009	FLAT CABLE 2X10 (9CM)	1
780891032	FLAT CABLE 2X20 (4 CONNECT)	1
780981003	FLAT CABLE 2X20 (3.5 CM)	1
780991608	FLAT CABLE 2X13 (8 CM)	1
CH599317010	STABILANT 22	1
LCLC9615	LOWER COVER WITH FEET	1
US9615	UPPER SHIELD AND ROD ASSY	1

RP9615: REAR PANEL ASSY

LeCroy Part Number	Description	Qty
315972600	RFI FILTER W/DBL FUSE BLOCK	1
433162630	FUSE SLO-BLO 250V 6.30AMP	2
469040002	*METAL BANANA JACK/BINDING POST	1
530409037	FINGER GUARD, 4.7" FAN	1
550010508	SCREW FLAT HEAD PHIL M3X8 W/NYLOCK	2
550431106	SCR PN HD PH W/WHR M3X6 W/NYLOCK	6
554035101	CLIP-ON NUT DIAM. 3.5	4
554435008	SCREW S/TAP PAN HD M3.5X16	4
577100002	WASHER SHAKEPROOF 1/4"	1
705740015	LABEL, PROTECTIVE GND SYMBOL	1
7093XX931	INTERF. HOLE CLOSURE 93XX-9	3
780834509	GROUND CABLE YELLOW/GREEN 9CM	1
785740005	LC574 LINE INPUT CABLE	1
F9301-4	GPIB + RS232 H-SPEED INTERFACE	1
F9601-2NY	CONNECTOR BOARD	1
F9602-9	FAN UNIVERSAL CONTROL. ASSY.	1
RP9615-9	REAR PANEL 9615-9	1

S9615-21: BUFFER BOARD

LeCroy Part Number	Description	Qty
454111050	HDR SOLD TAIL/MALE 50/STRAIGHT	1
71961521C	PC BD PREASSY 9615-21	1
SM232022822	DIODE ARRAY SCHOTTKY 2822	23
SM280120605	LOW POWER NMOSFET	2
SM281109430	P-CH ENHAN MOSFET SI9430	2
SM301302800	BEAD FERRITE Z=80 OHMS	21
SM301366561	INDUCTOR .56UH 10%	1
SM454520032	CONN HEADER RT ANGLE 32PIN SMT	1
SM455701005	CONNECTOR PCB/CABLE 5POS SMD	1
SM652101101	RES CHIP (E24) 1% 100 OHM	8
SM652101103	RES CHIP (E24) 1% 10 K	4
SM652101221	RES CHIP (E24) 1% 220 OHM	1
SM654101000	CHIP JUMPER ZERO OHMS	5
SM661207102	CAP CERA CHIP 20% .001 UF	4
SM661207103	CAP CERA CHIP 20% .01 UF	6
SM661207104	CAP CERA CHIP 20% .1 UF	1
SM667016106	CAP,TANT 10UF/16V 20%	1
SM668025106	CAP,TANT 10UF/25V 20% L ESR	4

S9615-22: INTERFACE CIRCUIT

LeCroy Part Number	Description	Qty
71961522A	PC BD PREASS'Y 9615-22	1
SM454520032	CONN HEADER RT ANGLE 32PIN SMT	1
SM455700031	*CONN DF9 RECEPTACLE 31 POS	1

S9615-51: KEYPAD

LeCroy Part Number	Description	Qty
256400105	LED YELLOW LOW CURRENT REAR MOUNT	1
454224030	HDR THIRD 41612 PRESSFIT FEM 30	1
71961551A	PC BD PREASS'Y 9615-51	1

S9615-52: GENERIC FRONT PANEL

LeCroy Part Number	Description	Qty
103427104	CAP CERA MONO 100V .1 UF	3
147436033	CAP ALUM METAL CAN 33 UF	1
161225471	RES CARBON FILM 470 OHMS	1
190042103	RESISTOR NETWORK 10 K	2
190642103	RESISTOR NETWORK 10 K	1
200331074	IC D-TYP FLOP 74HCT74	1
230020062	DIODE SWITCHING BAW62	30
425100024	ENCODER DIGITAL 24 POS	3
425101024	ENCODER DIGITAL 24 POS	8
454200030	HDR MALE THIRD 41612 TO FEM 30	1
454511020	HEADER RT ANGLE MALE 20	1
71961552B	PC BD PREASS'Y 9615-52	1
MFP414	IC MONO FRNT PANEL PROCESSOR MFP414	1

UC9615: UPPER COVER ASSEMBLY

LeCroy Part Number	Description	Qty
350150001	GASKET,ULTRAFLEX,PSA,6" X 0.25"DIA	3
350920024	MONEL MESH STRIP DIAM 2.4MM	70
550011120	SCREW PAN HEAD PHIL M4X20 W/NYLOCK	2
709600090	TIP-UP HANDLE	1
709615005	UPPER COVER	1

US9615: UPPER SHIELD AND ROD ASSY

LeCroy Part Number	Description	Qty
522011036	ADHESIVE TAPE 3.18X25MM	210
544420001	SPRING CPRSN 10.31MM ODX15.25 MMFL	1
550010706	SCREW ECO-FIX PHIL PAN M3X6 W/NYLOC	3
550431104	SCR PN HD PH W/WHR M3X4 W/NYLOCK	4
554525901	CLIP DIAM 3.1MM	1
709600810	9600-8 POWER SWITCH BUTTON	1
709600820	9600-8 POWER SWITCH ROD	1
709614310	RIGHT AIR COOLING GUIDE	1
709614320	LEFT AIR COOLING GUIDE	1
789615001	CONNECTOR ASSEMBLY 9615	1
F9601-8NY	MAIN SWITCH BOARD	1
US9615-3	UPPER SHIELD ASSY	1

8. Mechanical Parts

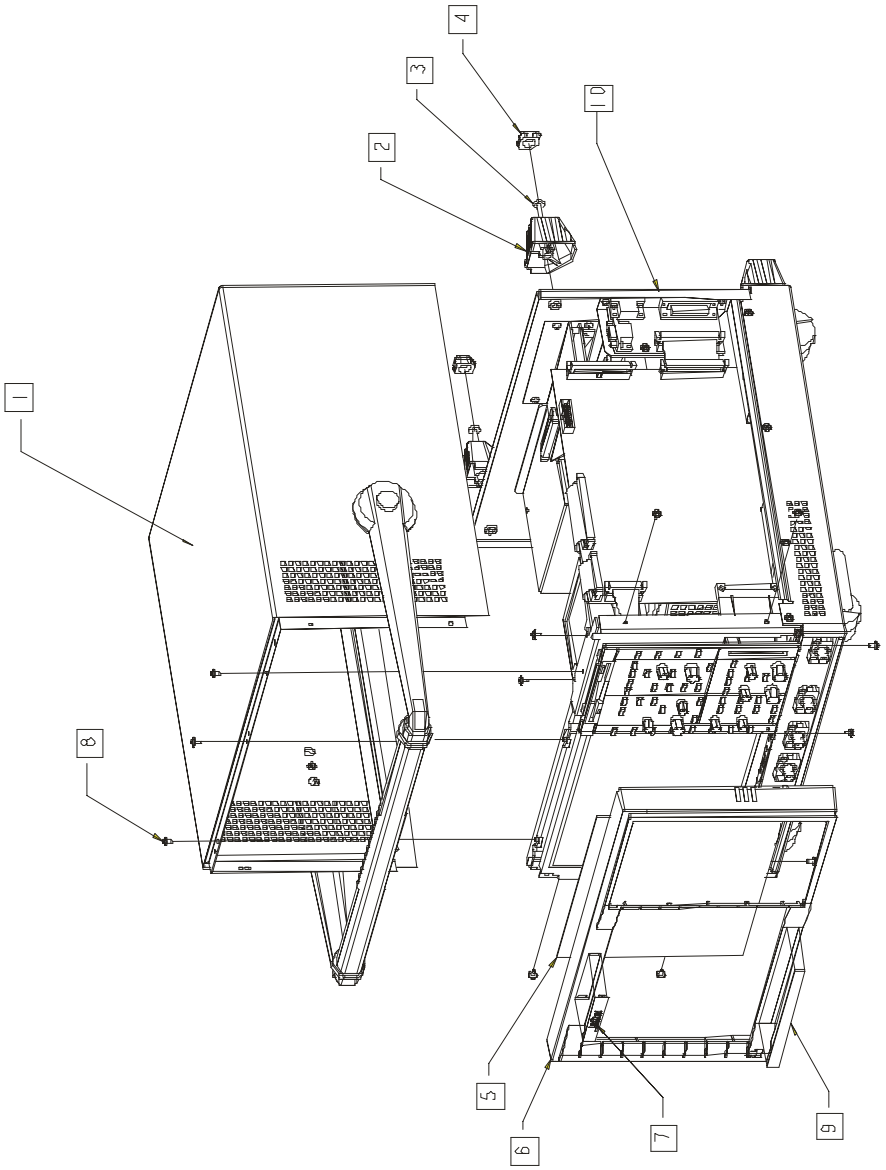


Figure 8-1: LC564DL Cabinet

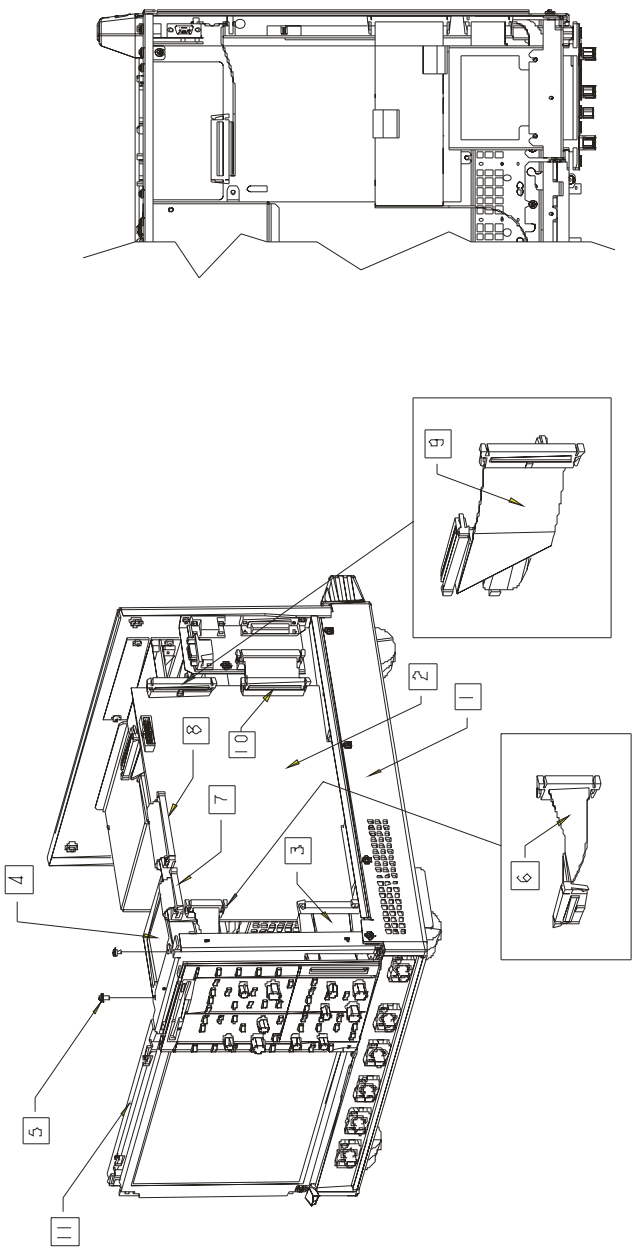


Figure 8-2: LC564DL Chassis Assembly

LC564DL Cabinet Replaceable Parts (Figure 8-1)

Item	LeCroy part Number	Qty	Description
1	UC9615	1	Upper Cover Assembly
2	709600075	4	9600 Rear Foot
3	550450116	4	Screw Cyl Hd Phil M5X16Mm
4	709600078	4	Rear Foot Rubber
5	709615201	1	Antiglare Glass Screen
6	709615000	1	Bezel Classic
7	709615010	1	Logo Lecroy For Flat Panel
8	550431106	10	Scr Pn Hd Ph W/Whr M3X6 W/Nylock
9	70LC55410	1	LC564DL Front Label

LC564DL Chassis Replaceable Parts (Figure 8-2)

Item	LeCroy Part Number	Qty	Description
1	LCXXX	1	Lower Cover Assembly
2	F9601-11-16	1	Color Up Card & 2X8Mb Dram
3	709424096	1	Memory Card Insert
4	F9601-61	1	Floppy Disk Drive Assy
5	550431106	2	Scr Pn Hd Ph W/Whr M3X6 W/Nylock
6	780721009	1	Flat Cable 2X10 (9Cm)
7	780991608	1	Flat Cable 2X13 (8 Cm)
8	780684001	1	Flat Cable 2X25 46Cm
9	780891032	1	Flat Cable 2X20 (4 Connect)
10	780981003	1	Flat Cable 2X20 (3.5 Cm)
11	LCDFP9615	1	LCD/Front Panel Assy

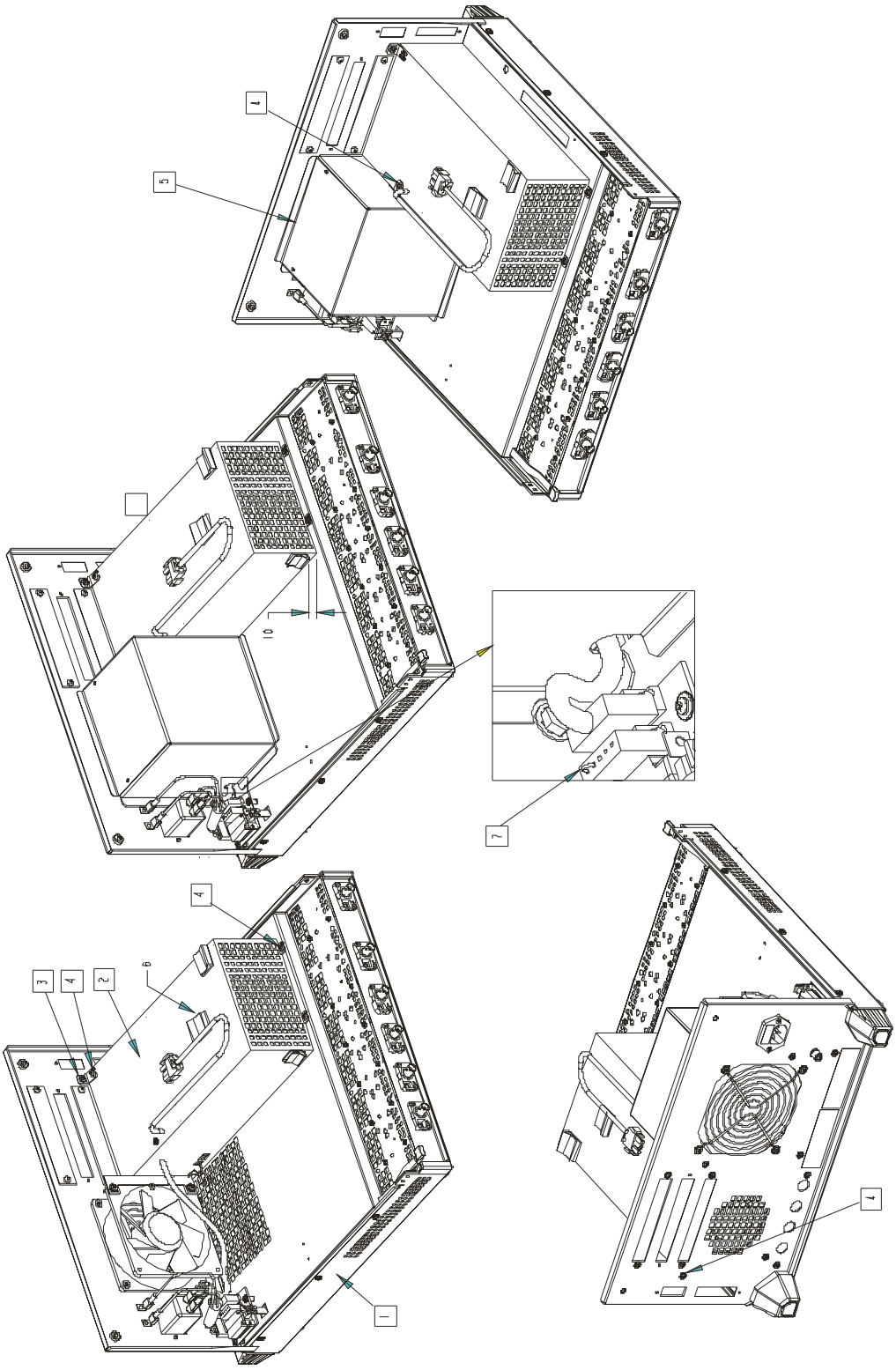


Figure 8-3 Power Supply Installation

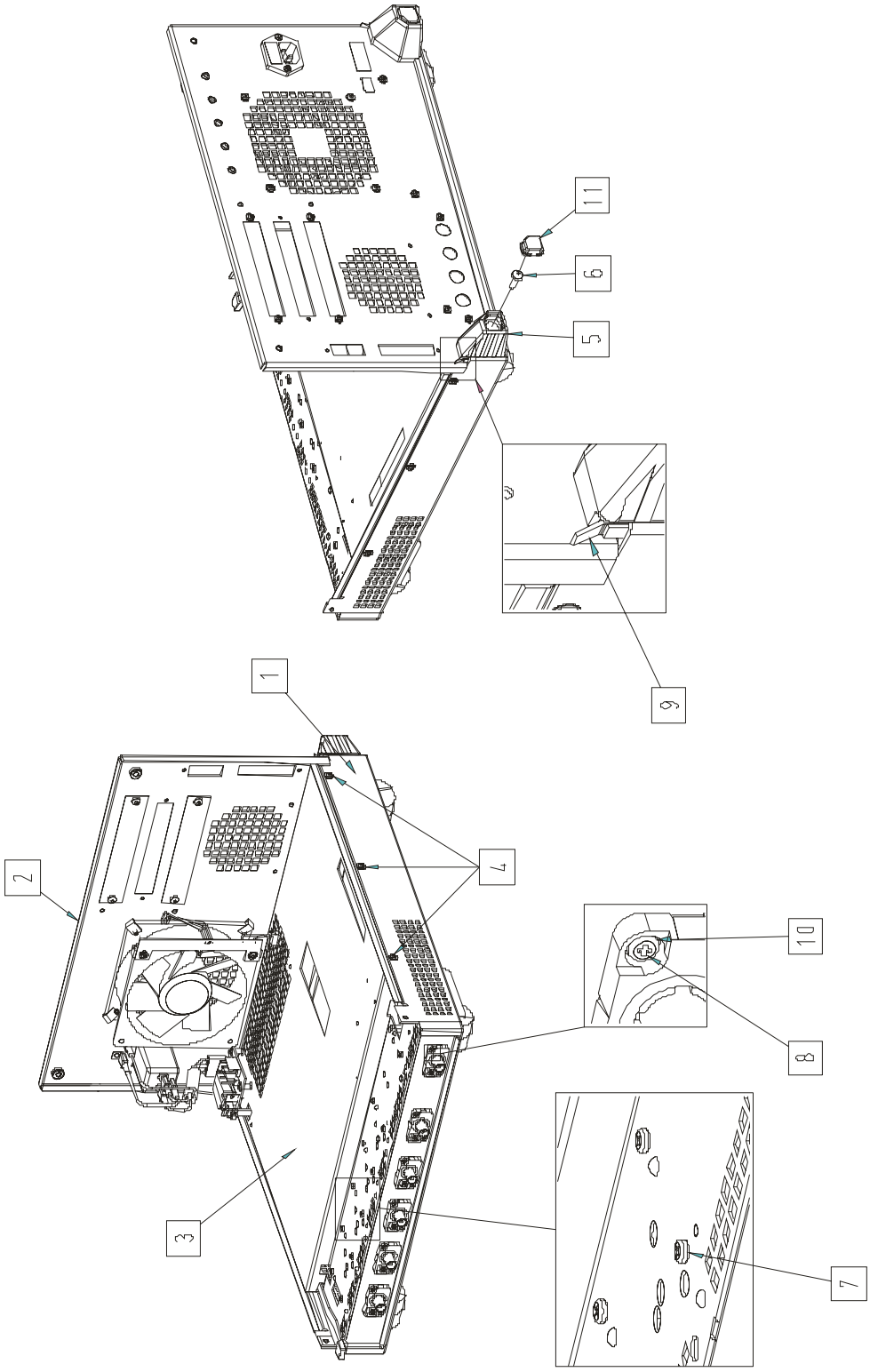


Figure 8-4: Lower Cover Assembly

Power Supply Installation Replaceable Parts(Figure 8-3)

Item	LeCroy Part Number	Qty	Description
1	LCLC9615	1	Lower Cover With Feet
2	PS9611	1	300W Power Supply
3	709614800	1	PS Square Angle Support
4	550431106	7	Scr Pn Hd Ph W/Whr M3X6 W/Nylock
5	709615901	1	Fan Chamber
6	594230002	3	Cable Clip Adhesive Back
7	789615001	1	Connector Assembly 9615

Lower Cover Replaceable Parts (Figure 8-4)

Item	LeCroy Part Number	Qty	Description
1	LCLC9615	1	Lower Cover With Feet
2	RP9615	1	Rear Panel Assy
3	US9615	1	Upper Shield And Rod Assy
4	550431106	6	Scr Pn Hd Ph W/Whr M3X6 W/Nylock
5	709600075	4	9600 Rear Foot
6	550450116	4	Screw Cyl Hd Phil M5X16Mm
7	550010130	12	Screw Pan Head Phil M3X30 W/Nylock
8	554425003	6	Screw S/Tap Phil M2.5X6 Black
9	709600048	2	9600 Upper Cover Lock Insert
11	709600078	4	Rear Foot Rubber

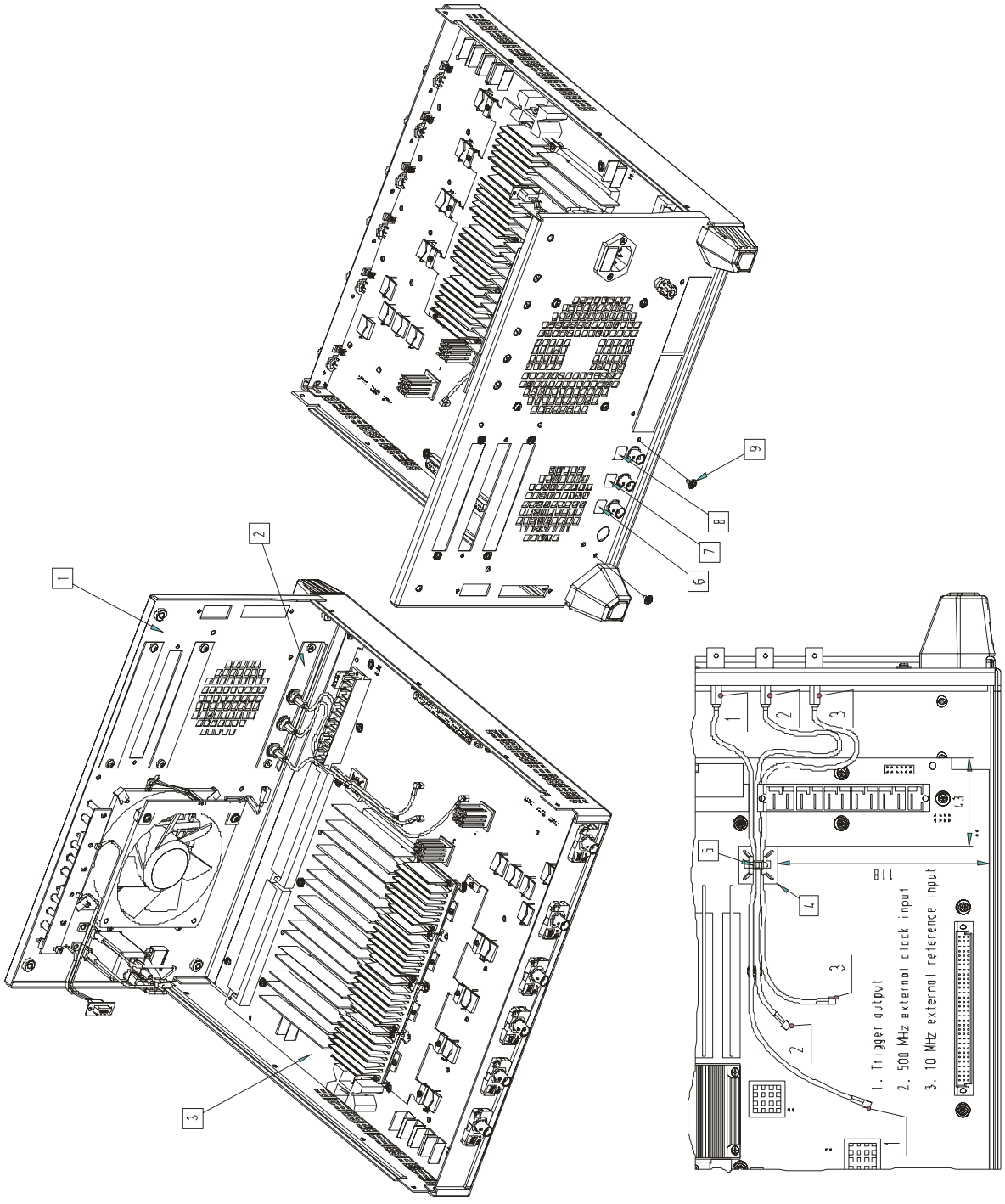


Figure 8-5: Lower Cover Assembly with CKTRIG Option

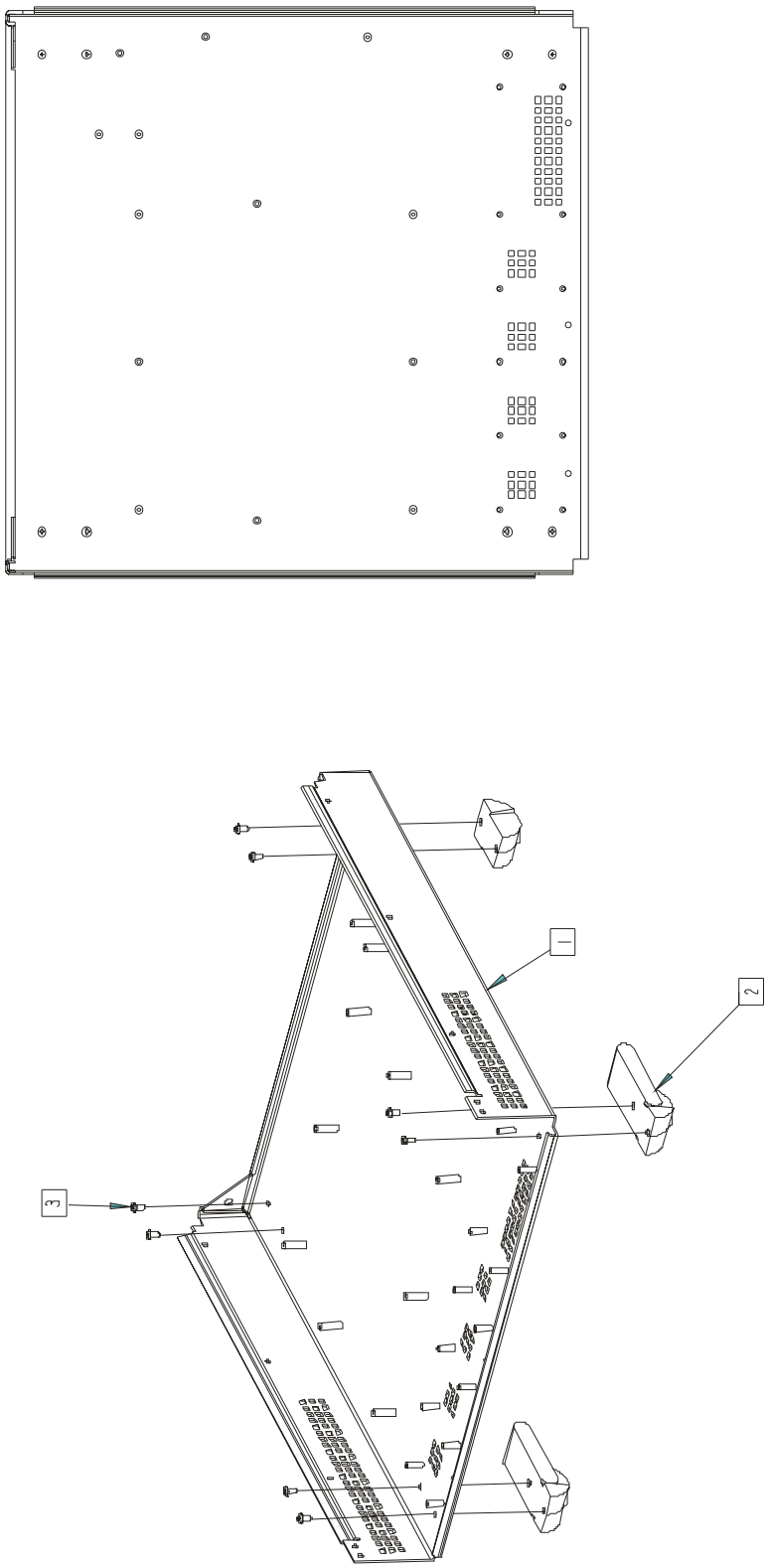


Figure 8-6: Lower Cover

Lower Cover with CKTRIG Option Replaceable Parts (Figure 8-5)

Item	LeCroy Part Number	Qty	Description
1	RP9615	1	Rear Panel Assy
2	LC684-CKTRIG	1	Clock And Trig Option
3	900079	1	Main Card Quad 4 Ghz
4	594150001	1	Tiewrap Base 3/4" Sq
5	594120003	1	Tiewrap
6	709350341	1	10Mhz Ext Ref Label
7	709350351	1	500Mhz Ext Clk Label
8	7096XX361	1	Trig Output Label
9	550431106	6	Scr Pn Hd Ph W/Whr M3X6 W/Nylock

Lower Cover Replaceable Parts (Figure 8-6)

Item	LeCroy Part Number	Qty	Description
1	709615305	1	Lower Cover
2	485325001	1	Set Of 4 Feet, Dark Grey
3	554435006	8	Screw S/Tap Pan Phil KA35X7

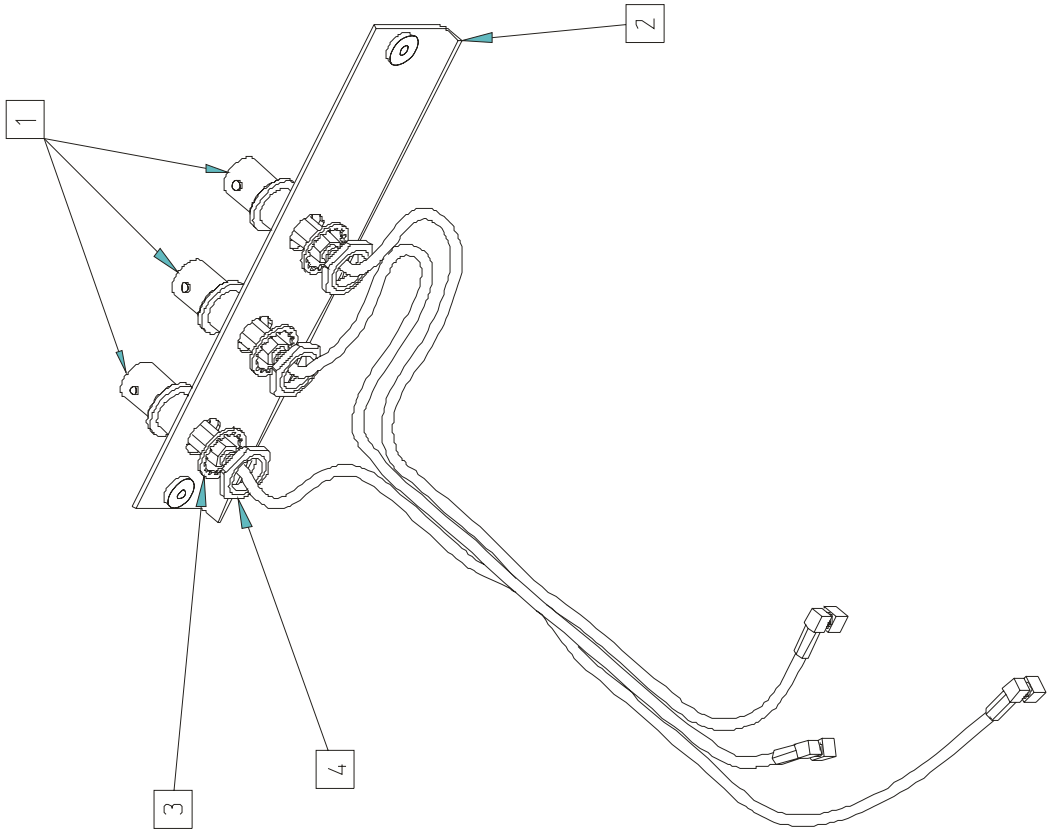


Figure 8-7: CKTRIG Option

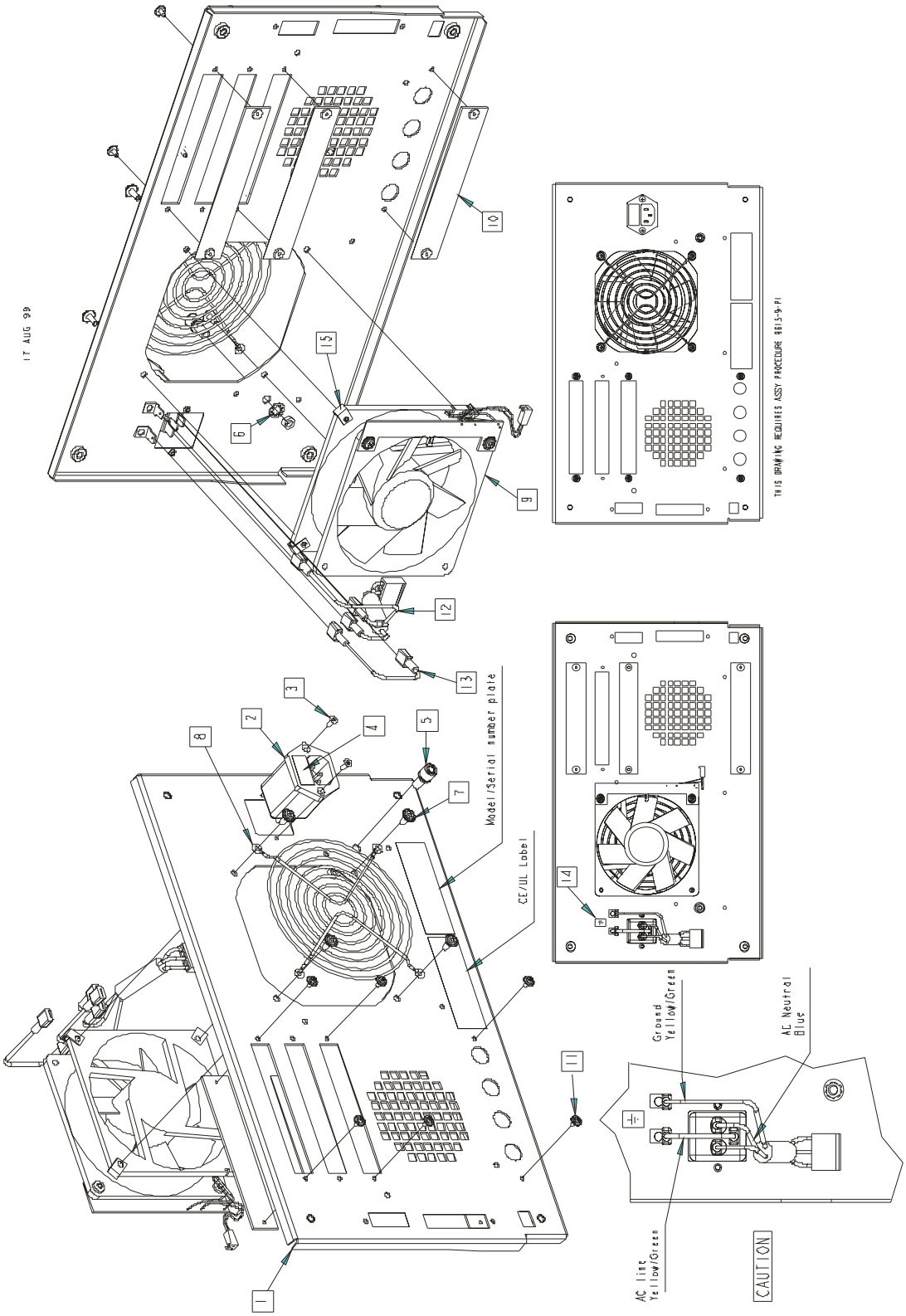


Figure 8-8: Rear Panel Assembly

CKTRIG Option Replaceable Parts (Figure 8-7)

Item	LeCroy Part Number	Qty	Description
1	781111128	3	Cable 28Cm RG316/U
2	709350331	1	935X-Cktrig Panel
3	709614301	3	Bnc Lockwasher
4	709614302	3	Bnc Nut

Rear Panel Replaceable Parts (Figure 8-8)

Item	LeCroy Part Number	Qty	Description
1	RP9615-9	1	Rear Panel 9615-9
2	315972600	1	Rfi Filter W/Dbl Fuse Block
3	550010508	2	Screw Flat Head Phil M3X8 W/Nylock
4	433162630	2	Fuse Slo-Blo 250V 6.30Amp
5	469040002	1	*Metal Banana Jack/Binding Post
6	577100002	1	Washer Shakeproof 1/4"
7	554435008	4	Screw S/Tap Pan Hd M3.5X16
8	530409037	1	Finger Guard, 4.7" Fan
9	F9602-9	1	Fan Universal Control. Assy.
10	7093XX931	3	Interf. Hole Closure 93XX-9
11	550431106	6	Scr Pn Hd Ph W/Whr M3X6 W/Nylock
12	785740005	1	Lc574 Line Input Cable
13	780834509	1	Ground Cable Yellow/Green 9cm
14	705740015	1	Label, Protective Gnd Symbol
15	554035101	4	Clip-On Nut Diam. 3.5

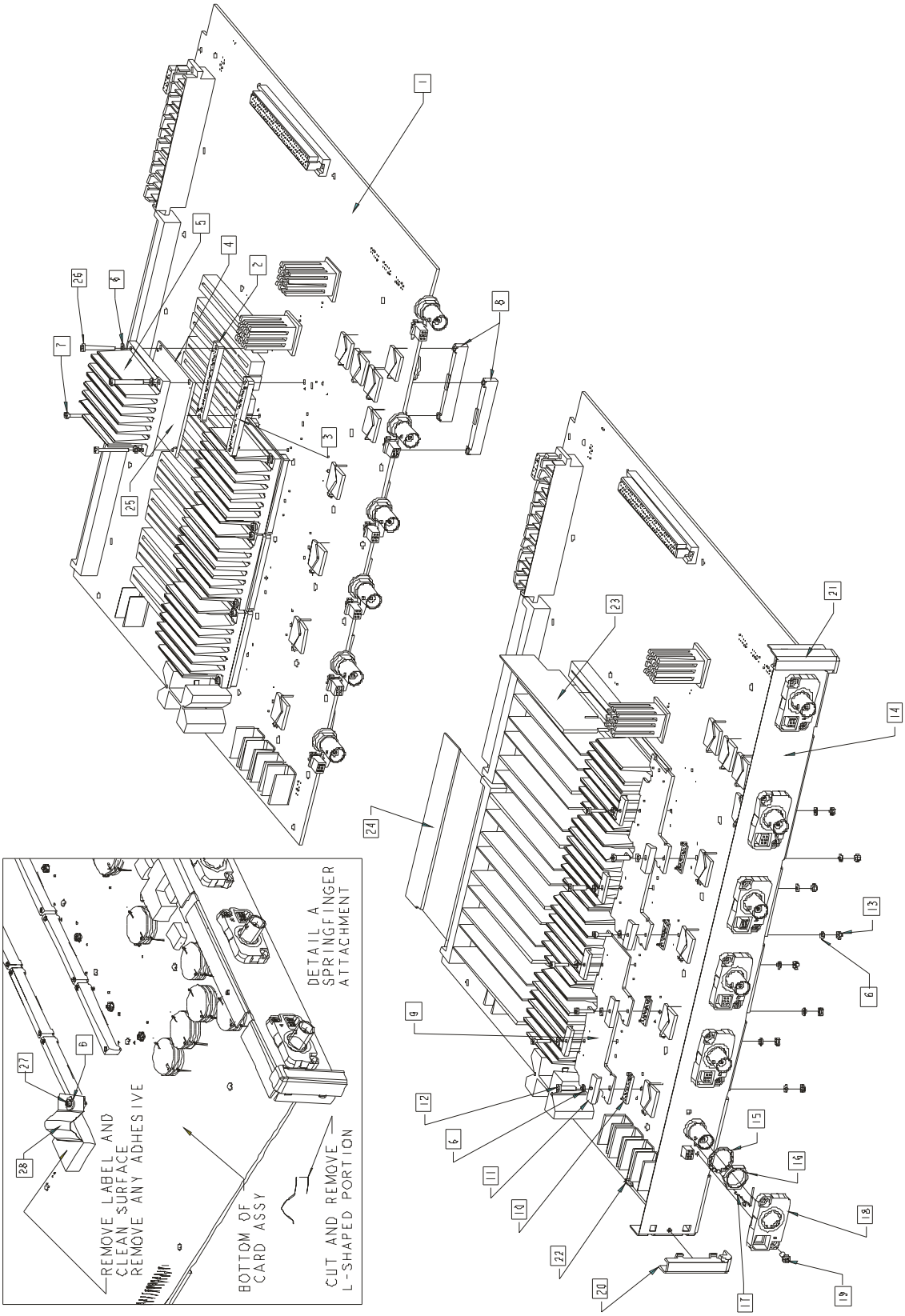


Figure 8-9: 900079 Main Board Assembly

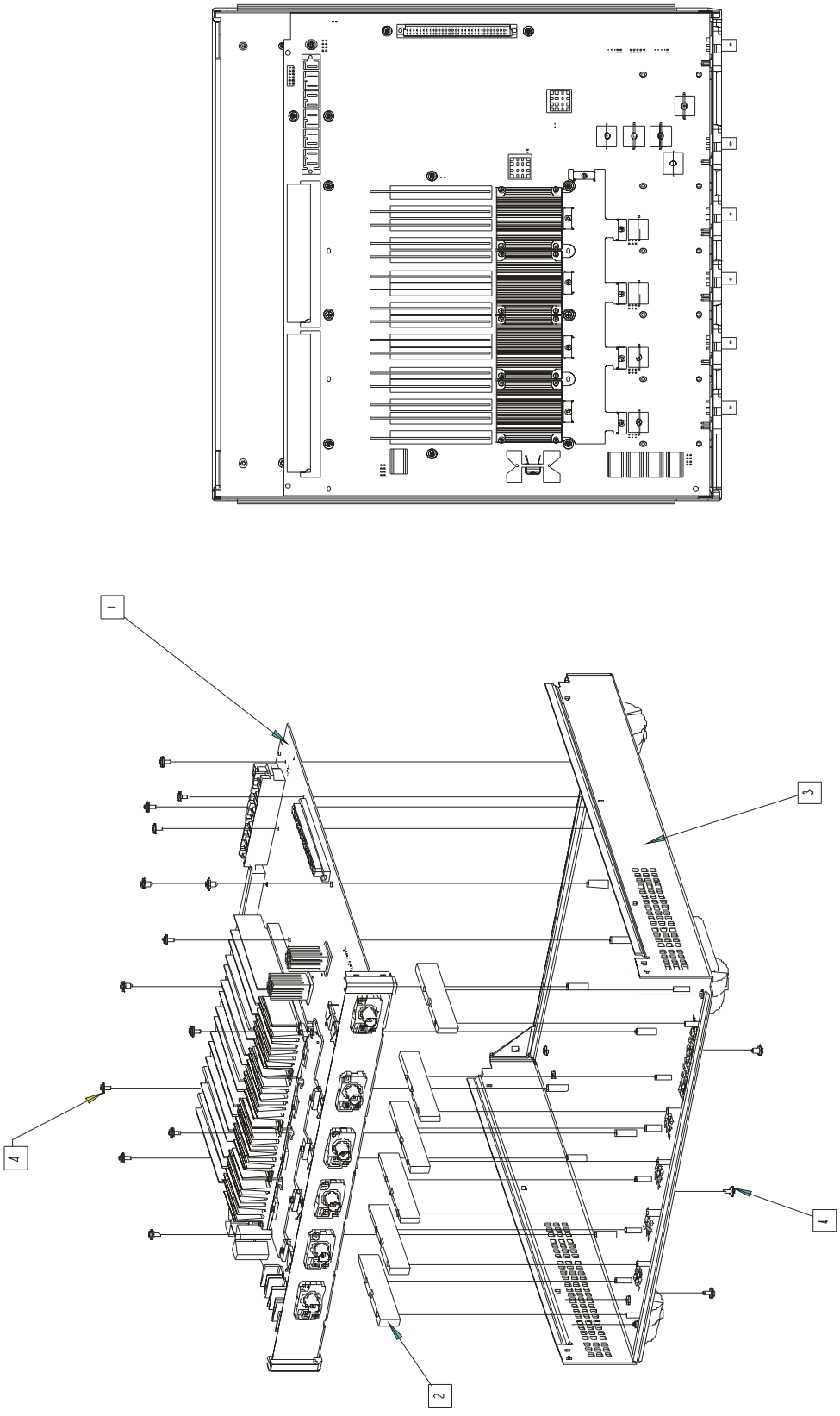


Figure 8-10: 900079 Main Board Assembly

900079 Main Board Replaceable Parts (Figure 8-9)

Item	LeCroy Part Number	Qty	Description
1	S9615-3	1	Main Card Quad 4 Ghz
2	SM454213064	4	Conn Cin:Apse 64 Pts 3.5mm
3	SM454213056	4	Conn Cin:Apse 56 Pts 3.5mm
4	HAM435	4	2Gs/S Acq. Module
5	709614321	4	HAM421 Heatsink
6	551420400	33	Washer Shakeproof M2
7	550420820	15	Screw Cyl Hd Phil M2X20
8	709614315	8	HAM421 Tightener
9	HSY430	2	Switch Yard Board HSY430
10	SM454213016	8	Conn Cin:Apse 16 Pts 1.4mm
11	709614312	8	HSY 425 Tightener
12	550420110	8	Screw Cyl Hd Phil M2X10mm
13	552420100	8	4mm Hex Nut M2 Thd
14	FP9615-3	1	Main Card Panel 9615-3
15	709614301	6	Bnc Lock Washer
16	709614302	6	Bnc Nut
17	7093XXP91	6	Probe Ring Contact
18	7093XXP41	6	Probe Holder
19	554425003	6	Screw S/Tap Phil M2.5X6 Black
20	709600024	1	9600 Left Hub Cap
21	709600020	1	9600 Right Hub Cap
22	554422006	2	Screw S/Tap Pan Phil KA22X5
23	HMM436S	16	*Acquisition Mem. Module 2 Mbit
24	205800234	2	*2M X 32 Dram Module
25	CH599041022	1	Heat Sink Compound 251
26	550120116	1	Screw Pan Hd Ph M2X16 St Stl Pass
27	550120104	1	Screw Pan Hd Hp M2X4 St Stl Pass
28	350351001	0	Gasket, Shielding, Clip-On

900079 Main Board Replaceable Parts (Figure 8-10)

Item	LeCroy Part Number	Qty	Description
1	900080	1	Main Card Quad 4 Ghz
2	709614340	6	9614 Shield Lower Partition
3	LCLC9615	1	Lower Cover With Feet
4	550431106	13	Scr Pn Hd Ph W/Whr M3X6 W/Nylock

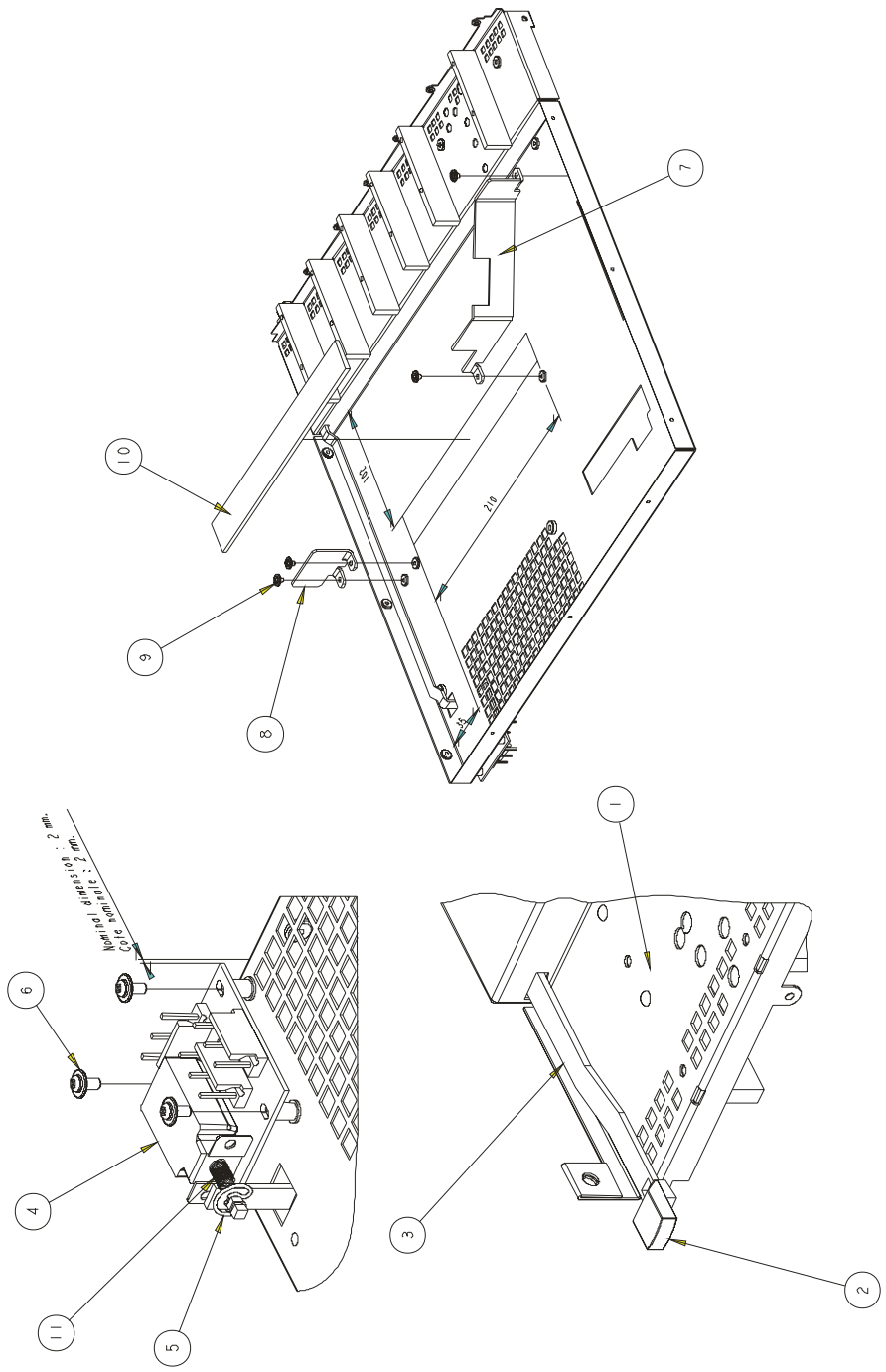


Figure 8-11: Upper Shield Assembly

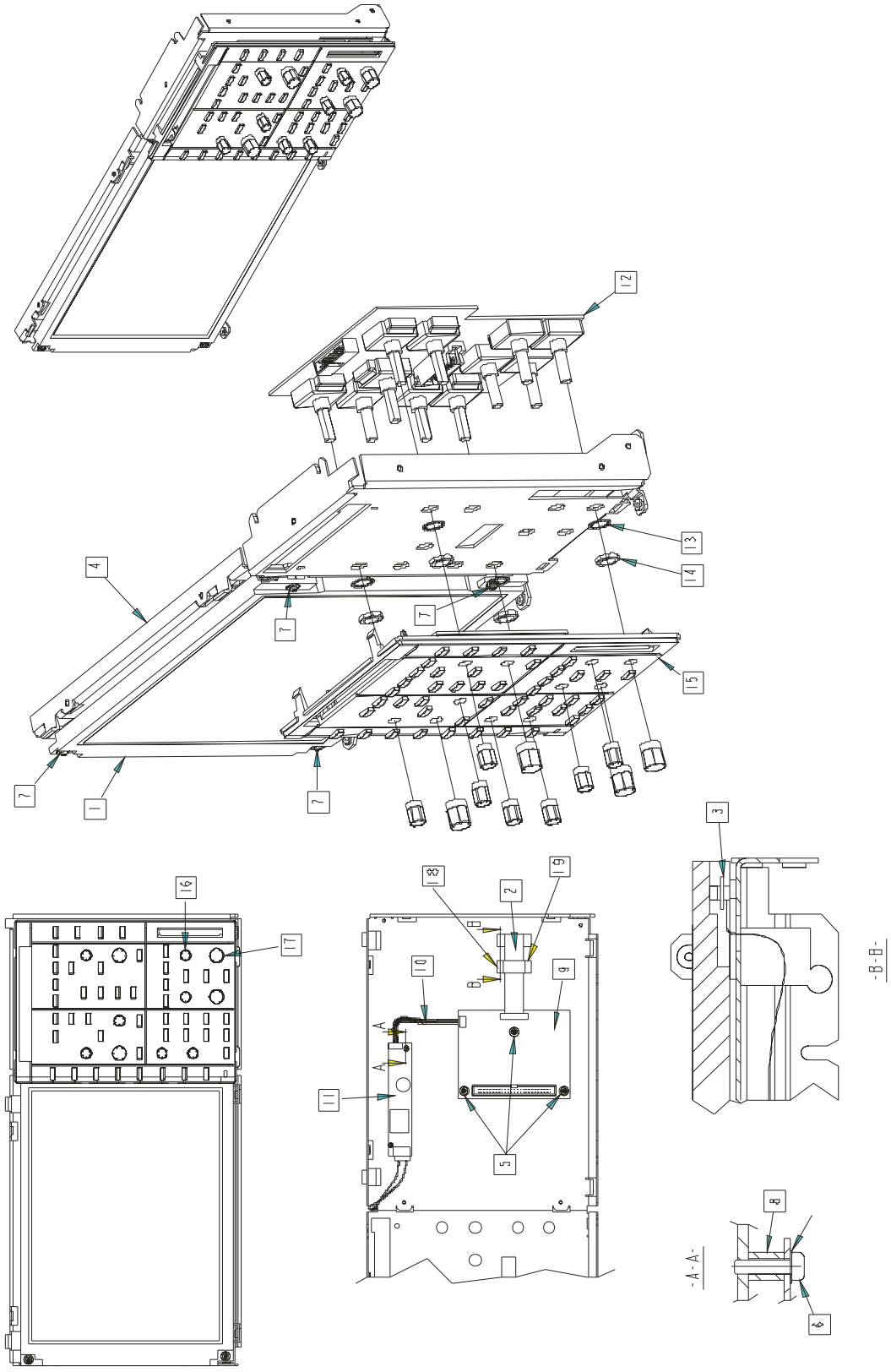


Figure 8-12: Front Frame Assembly

Upper Shield Replaceable Parts (Figure 8-11)

Item	LeCroy Part Number	Qty	Description
1	US9615-3	1	Upper Shield Assy
2	709600810	1	9600-8 Power Switch Button
3	709600820	1	9600-8 Power Switch Rod
4	F9601-8	1	Main Switch Board
5	554525901	1	Clip Diam 3.1Mm
6	550010706	3	Screw ECO-Fix Phil Pan M3X6 W/Nylock
7	709614310	1	Right Air Cooling Guide
8	709614320	1	Left Air Cooling Guide
9	550431104	4	Scr Pn Hd Ph W/Whr M3X4 W/Nylock
10	522011036	210	Adhesive Tape 3.18X25Mm
11	544420001	1	Spring Cmprsn 10.31MM ODx15.25 MMFL

Front Panel Replaceable Parts (Figure 8-12)

Item	LeCroy Part Number	Qty	Description
1	258104001	1	TFT Color Lcd Module, 10.4 Inch
2	592000032	1	Flat Cable 32 Pos .5 Step
3	S9615-22	1	Interface Circuit
4	709615007	1	Front Frame (Sharp)
5	550430706	3	Screw Eco-Fix M3X6
6	550420108	2	Screw Pan Hd Phil M2.0X8mm Lg
7	550430608	4	*Screw Eco-Fix M3X8
8	520200120	2	Spacer 4mmodx2.6mmidx5mmlg Nylon Bk
9	S9615-21	1	Buffer Board
10	300070000	1	Ferrite Shielding Flat Cable
11	315000003	1	Tft Dc-Ac Inverter Unit
12	F9615-5	1	Keyboard Assy
13	551090001	4	M9 Lockwasher
14	552090075	4	M9 X 0.75 Mounting Nut
15	S9615-52	1	Generic Front Panel
16	709600560	7	9600-5 Knob Diam 9
17	709600570	4	9600-5 Knob Diam 12

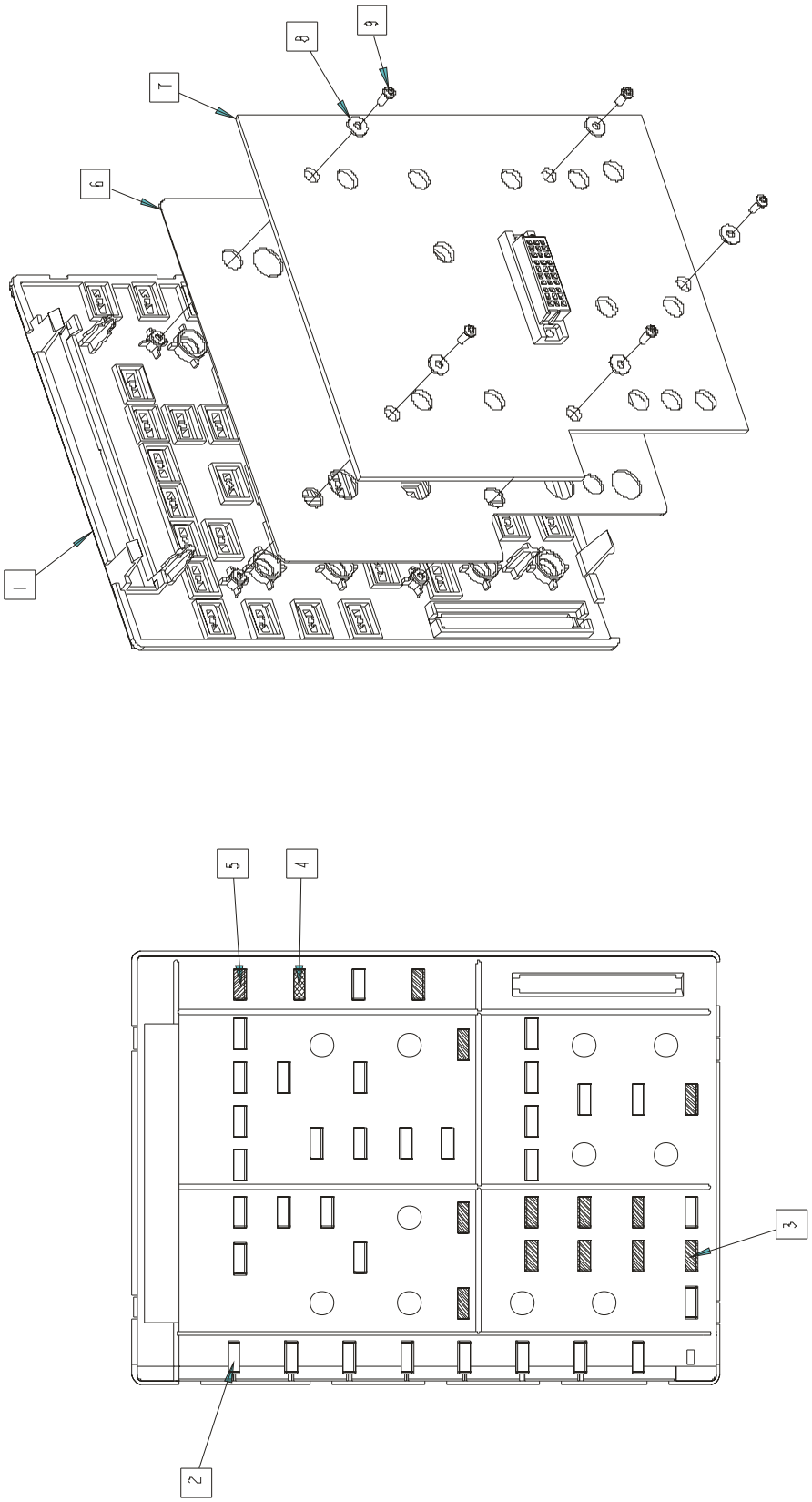


Figure 8-13: Keypad Assembly

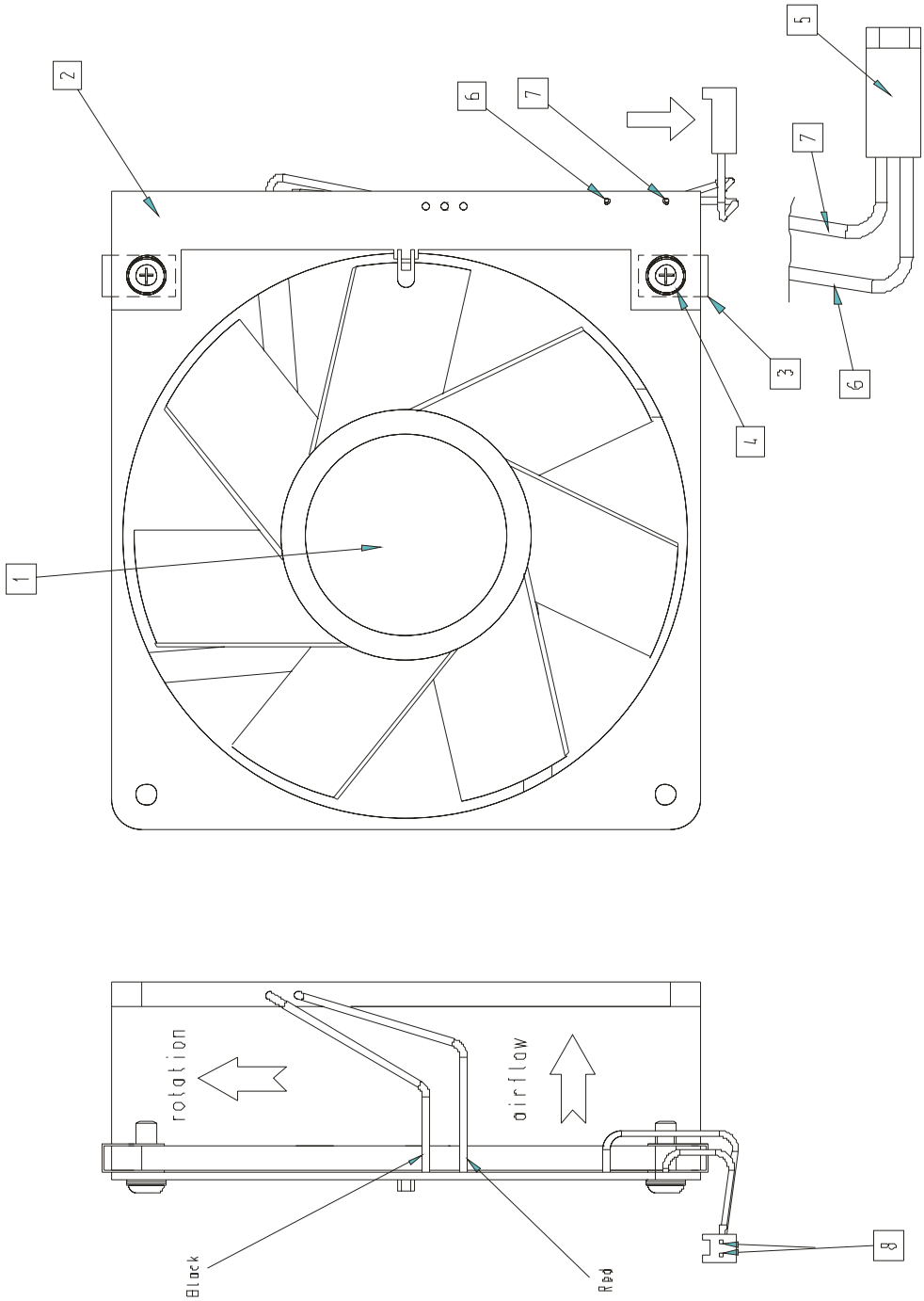


Figure 8-14: Fan Assembly

Keypad Replaceable Parts (Figure 8-13)

Item	LeCroy Part Number	Qty	Description
1	709615512	1	Front Panel Classic
2	709600510	32	9600-5 Switch Cap, Light Grey
3	709600512	12	9600-5 Switch Cap Dark Grey
4	709600516	1	9600-5 Switch Cap, Green
5	709600514	1	9600-5 Switch Cap, Blue
6	709615500	1	TFT Rubber Mat
7	S9615-51	1	Keypad
8	551423100	5	Flat Washer M2.3
9	554422005	5	Screw S/Tap Pan Phil KA22X6

Fan Replaceable Parts (Figure 8-14)

Item	LeCroy Part Number	Qty	Description
1	530409116	1	12V DC Fan, Brushless
2	S9602-9	1	Fan Universal Control. Circuit
3	554035101	2	Clip-On Nut Diam. 3.5
4	554010013	2	Screw S/Tap Pan Hd M3.5X13
5	405154002	1	Conn Housing 2-Pos
6	590221022	1	Wire Teflon 7/30 Red 22
7	590001022	1	Wire Teflon 7/30 Blk 22
8	405708001	2	Terminal Anti-Fishhooking Crimp

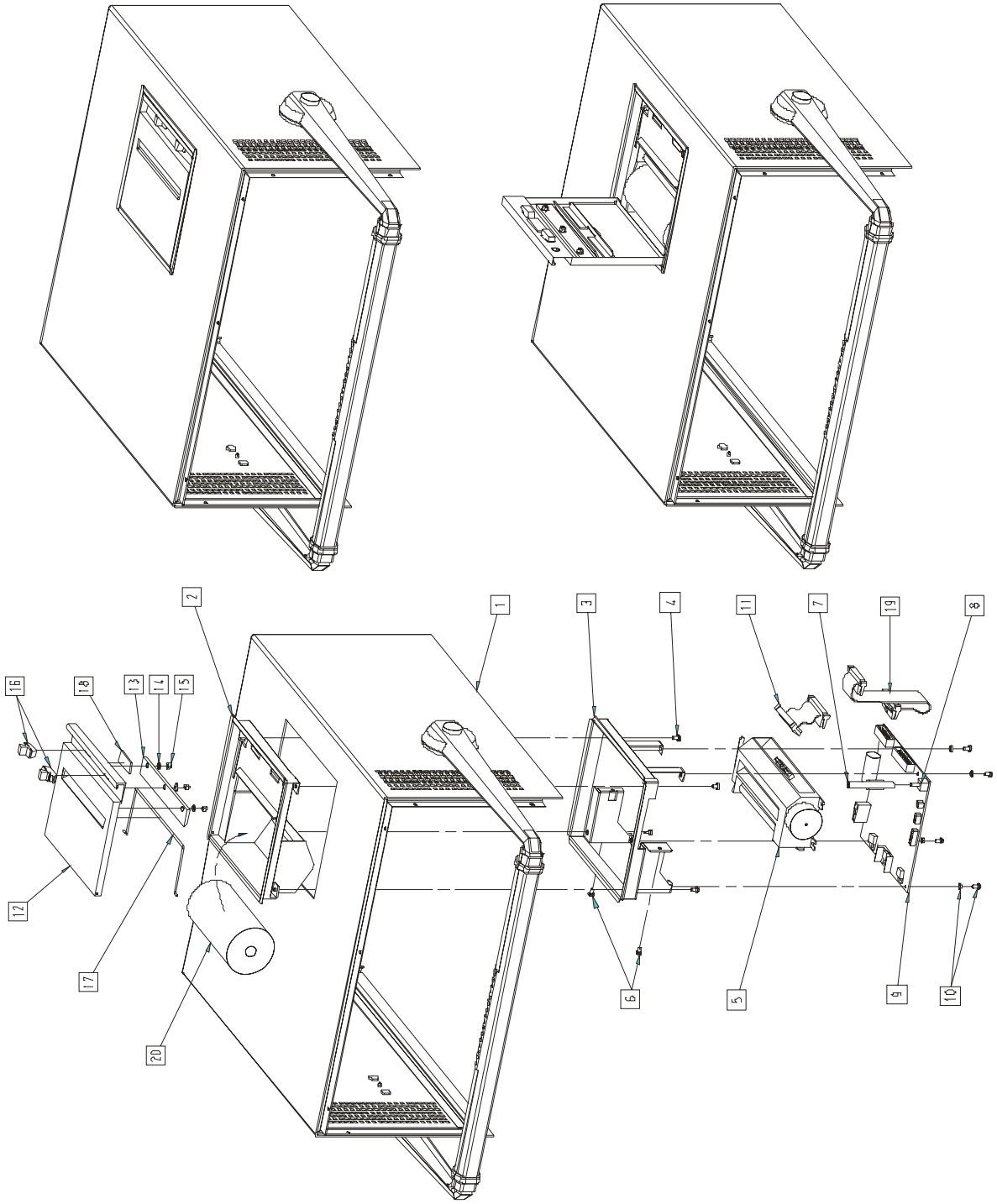


Figure 8-15: Graphic Printer Assembly

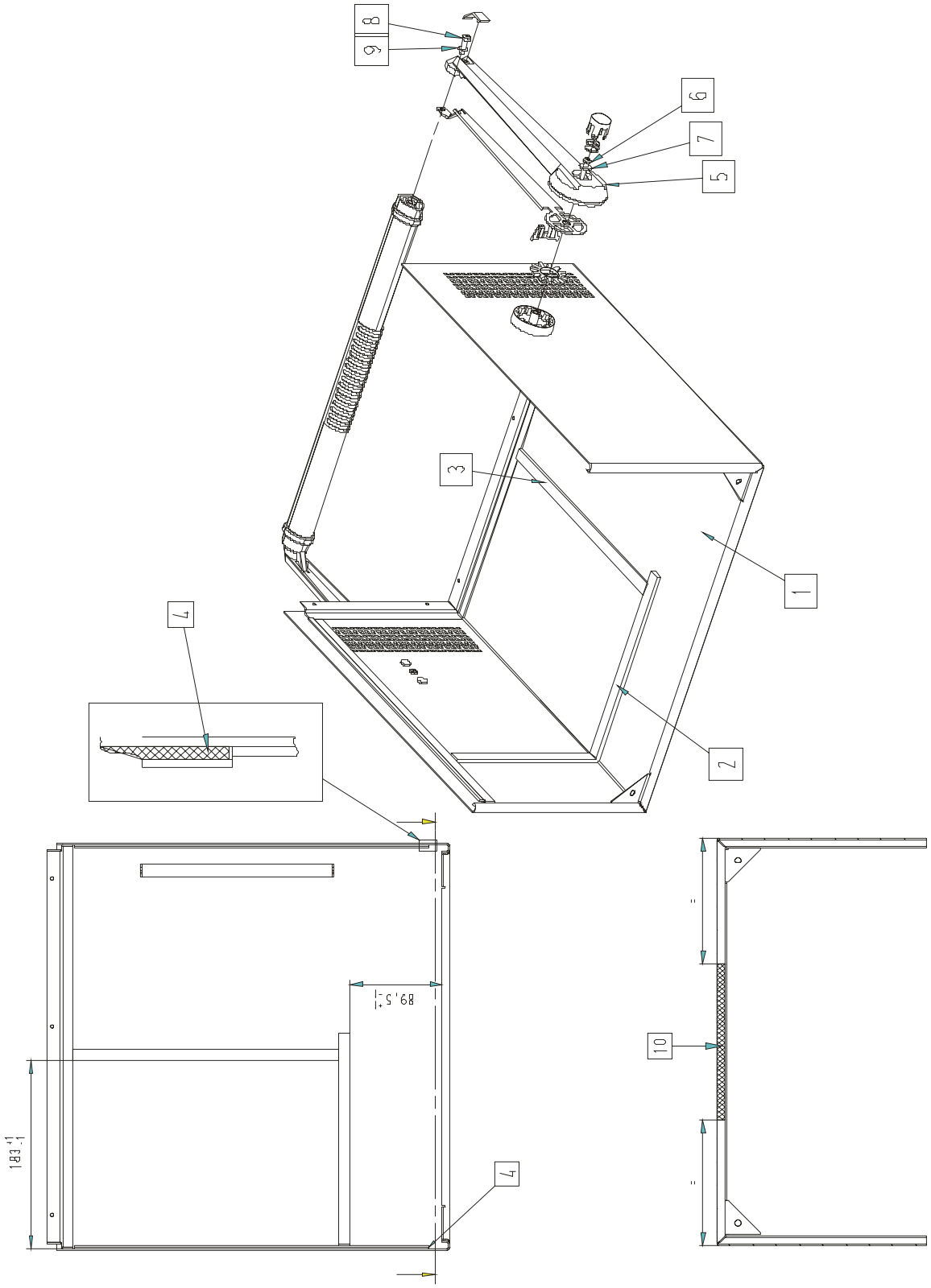


Figure 8-16: Upper Cover Assembly

Graphic Printer Replaceable Parts (Figure 8-15)

Item	LeCroy Part Number	Qty	Description
1	709615006	1	GP01 Upper Cover
2	BOX-GP01	1	GP01 Graphic Printer Box
3	709601031	1	Graphic Printer Frame
4	550010106	4	Screw Pan Head Phil M3X6 W/Nylock
5	334000832	1	Thermal Printer Unit
6	550011120	2	Screw Pan Head Phil M4X20 W/Nylock
7	70GP01061	1	Graphic Printer Switch Button
8	709450523	1	Push Switch Extender
9	F9300-7	1	LTP 5446 Printer Controller
10	550010105	7	Screw Pan Head Phil M3X5 W/Nylock
11	780791604	1	Flat Cable 2X13 (4cm)
12	COVER-GP01	1	GP01 Graphic Printer Cover
13	70GP01051	1	Graphic Printer Cutter
14	551430100	3	Flat Washer M3
15	552430300	3	Nut Open-End Acorn M3
16	530040005	2	Slide Latch Tab Style
17	70GP01041	1	Graphic Printer Cover Axle
18	389340008	30	Auto-Adhesive Rubber Band 12X2mm
19	780721022	1	Flat Cable 2X10 (22cm)
20	334000402	1	Thermal Paper For Seiko Printer
21	709600090	1	Tip-Up Handle

Upper Cover Replaceable Parts (Figure 8-16)

Item	LeCroy Part Number	Qty	Description
1	709615005	1	Upper Cover
2	350920024	70	Monel Mesh Strip Diam 2.4Mm
3	709600090	1	Tip-Up Handle
4	350150001	3	Gasket,Ultraflex,Psa,6" X 0.25"Dia
5	709600090 kit	2	Arm
6	550011120	2	Screw Pan Head Phil M4X20 W/Nylock
7	709600090 kit	2	Flat Washer M4
8	709600090 kit	2	Socket Head Screw M5X16 Loctite Coated
9	709600090 kit	2	Washer M5
10	350150001	3	Gasket,Ultraflex,PSA,6" X 0.25"Dia

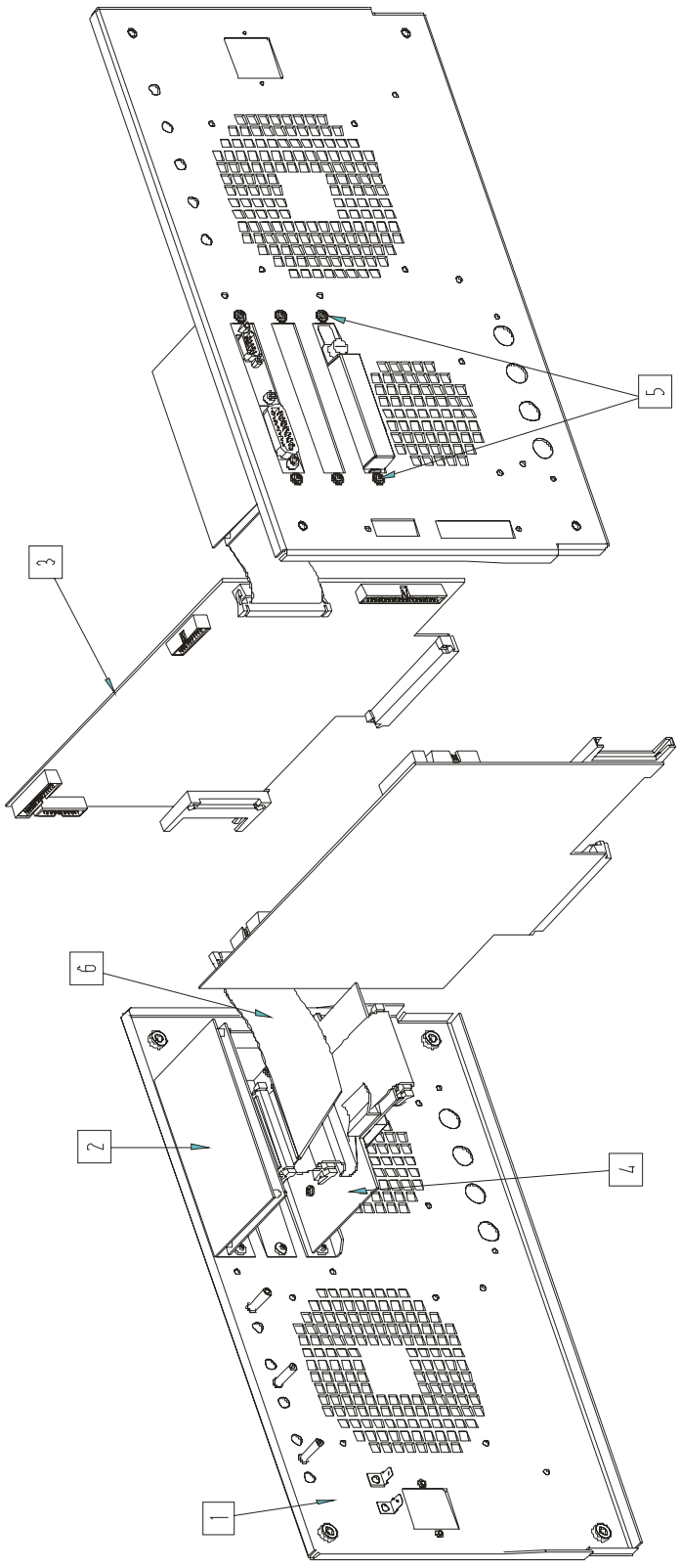


Figure 8-17: Hard Disk Assembly

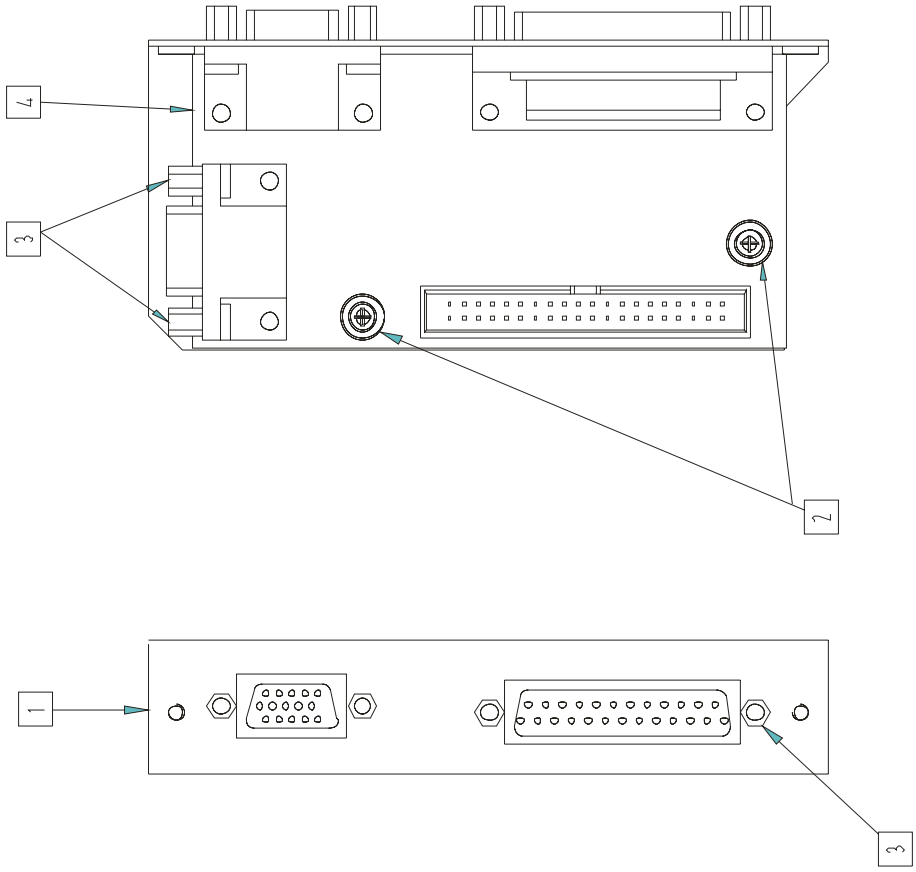


Figure 8-18: Centronics & VGA Interface Assembly

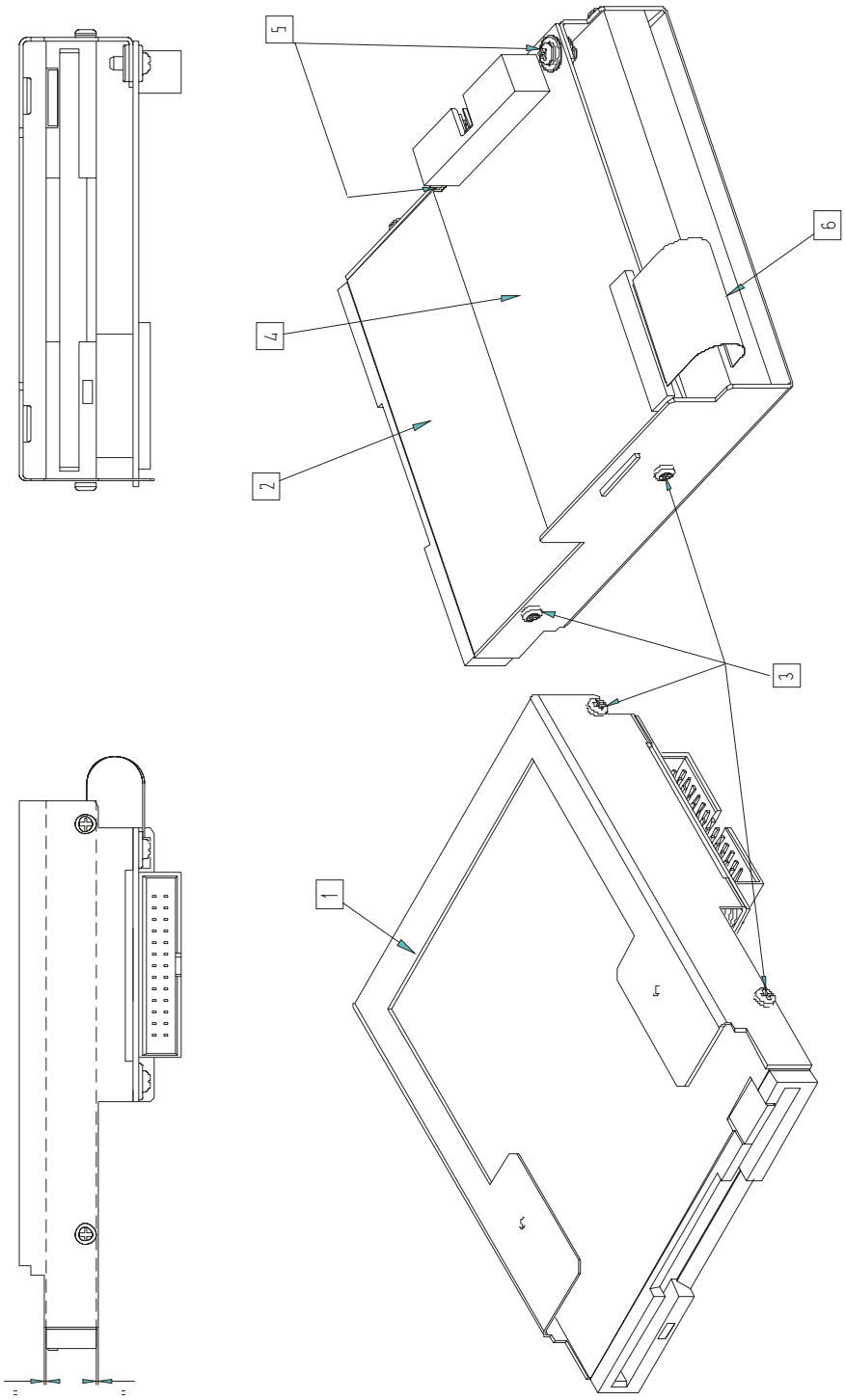


Figure 8-19: Floppy Disk Assembly

Hard Disk Replaceable Parts (Figure 8-17)

Item	LeCroy Part Number	Qty	Description
1	RP9615-9	1	Rear Panel
2	F9301-4	1	GPIB & RS232 Interface
3	F9601-11-16	1	Processor Card
4	F9300-8	1	PCMCIA III Controller Assembly
5	550010706	2	Screw eco-fix M3X6 w / Nylock
6	780891032	1	Flat cable 2X20 (4 connect)

Centronics & VGA Replaceable Parts (Figure 8-18)

Item	LeCroy Part Number	Qty	Description
1	709601211	1	Bracket
2	550431106	2	Screw pan hd PH w/whr M3X6 w / Nylock
3	405204000	6	Mounting hdw for conn.shell
4	F9601-2	1	Centronics & VGA Card

Floppy Replaceable Parts (Figure 8-19)

Item	LeCroy Part Number	Qty	Description
1	709600611	1	Floppy Drive support
2	330000002	1	Floppy Disk Drive 3.5”
3	550010103	4	Screw pan hd phil M2.5X3 w/ Nylock
4	S9601-61	1	Interface Card
5	550010706	2	Screw eco-fix M3X6 w / Nylock

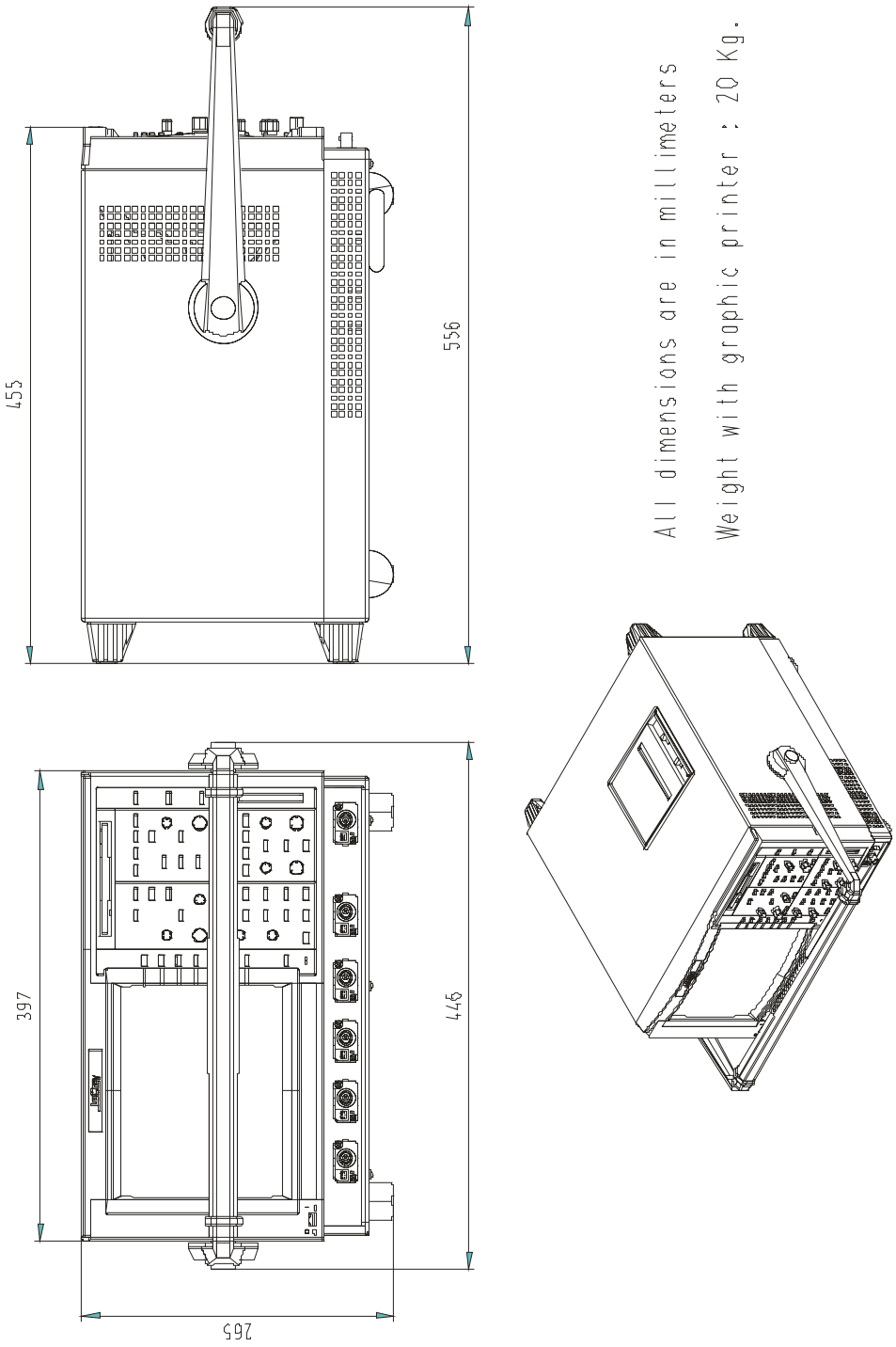


Figure 8-20: LC564DL Dimensions

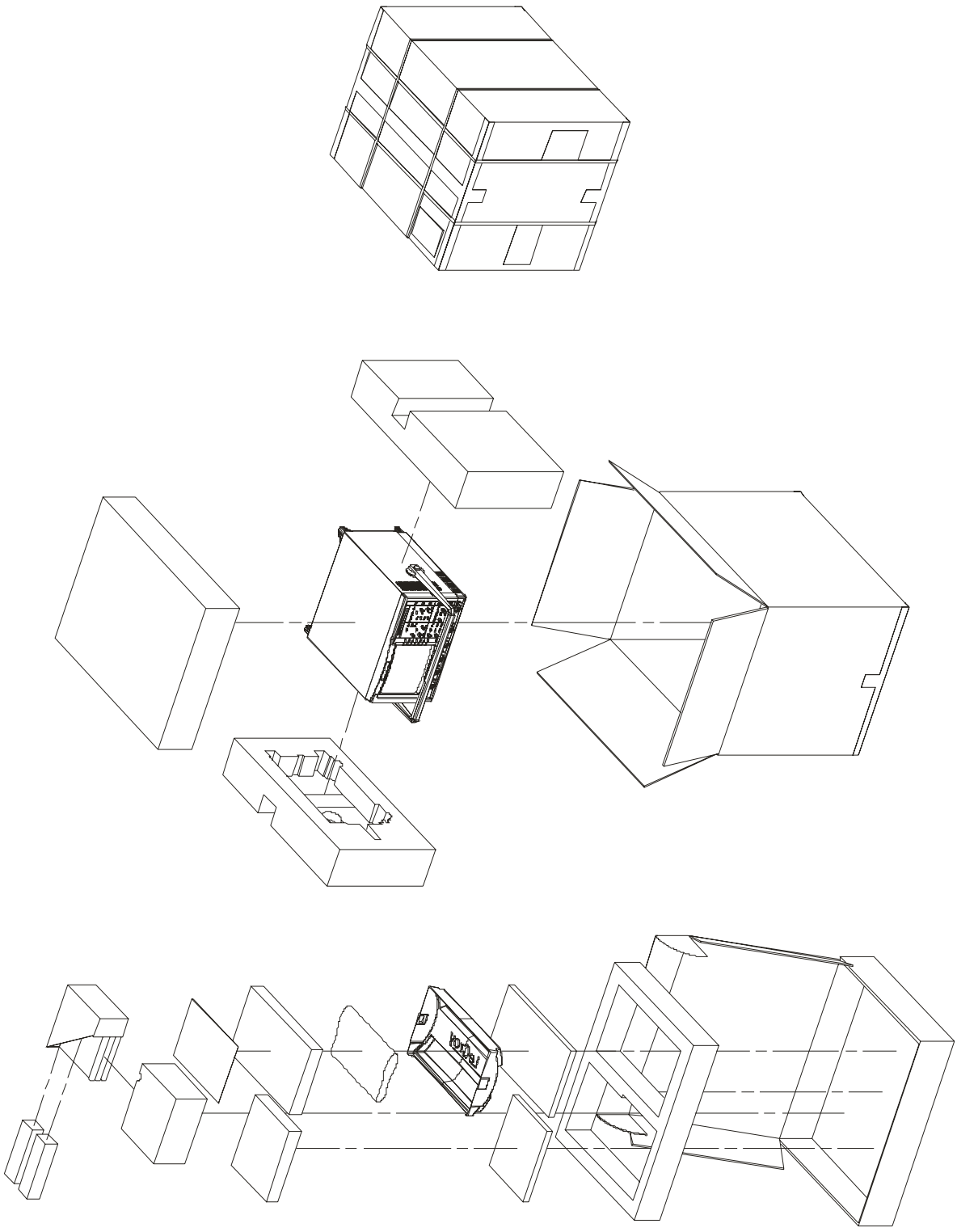


Figure 8-21: LC564DL Packaging